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PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Appl. No.	:	09/351,521	Confirmation No.9839
Applicant	:	Fumihiro Muramatsu et al.	
Filed	:	July 12, 1999	
TC/A.U.	:	2684	
Examiner	:	Tilahun Gesesse	
Docket No.	:	31879	
Customer No.	:	00116	

#18

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Commissioner for Patents
P.O. Box 1450
Alexandria, Va. 22313-1450

RULE 313 PETITION
TO WITHDRAW PATENT APPLICATION FROM ISSUE
AFTER PAYMENT OF ISSUE FEE

Sir:

Applicant hereby petitions and requests that the above-identified patent application be withdrawn from issue pursuant to 37 CFR § 1.313(c)(2). In accordance with 37 CFR § 1.313(a), applicant's petition is supported by good and sufficient reasons why withdrawal of the application from issue is necessary, as follows. Please charge the required $130 petition fee set forth in § 1.17(h) to Deposit Account No. 16-0820, Order No. 31879.

Applicant and its representatives became aware of the existence an additional document which required submission under 37 C.F.R. § 56 but which was inadvertently submitted without the requisite statement required by 37 C.F.R. §1.97(e)(1), and thus must be resubmitted with an

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Amy L. Hunt
Name of person signing certification

08 March 2004 Amy L. Hunt
Date Signature

RCE to be considered. This document is believed to be sufficiently relevant to warrant entry into the record in this application and consideration by the Examiner.

A Request for a Continued Examination (RCE) and an Information Disclosure Statement including Form PTO-1449 is filed herewith.

If there are any additional fees resulting from this communication, please charge same to our Deposit Account No. 16-0820, our Order No. 31879.

Respectfully submitted,

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08 March 2004

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#20

SUBMISSION OF SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

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Sir:

In accordance with 37 C.F.R. § 1.97(b)(4), applicant is submitting herewith Form PTO-1449 listing references for consideration by the Examiner. Also submitted herewith is a legible copy of each reference listed.

If there are any fees required by this communication, please charge the same to Deposit Account No. 16-0820, Order No. 31879.

Respectfully submitted,
Pearne & Gordon LLP

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March 8, 2004

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Form PTO-1449	U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY. DOCKET NO. 31879	SERIAL NO. 09/351,521
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		FILING DATE: July 12, 1999	GROUP ART UNIT: 2684

U.S. PATENT DOCUMENTS

Examiner Initial		Document No.	Date	Name	Class	Subclass	Filing Date If Appropriate
	A			RECEIVED			
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	C						
	D			OFFICE OF PETITIONS			
	E						
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	G						
	H						
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FOREIGN PATENT DOCUMENTS

		Document No.	Date	Country	Class	Subclass	Translation
	L	WO 92/15073	09/1992	PCT			English Text
	M	0 601 820 A1	06/1994	European			English Text
	N	WO 93/25955	12/1993	PCT			English Text
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	Q						

OTHER REFERENCES *(Including Author, Title, Date, Pertinent Pages, Etc.)*

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*Examiner: Initial if reference considered, regardless of whether citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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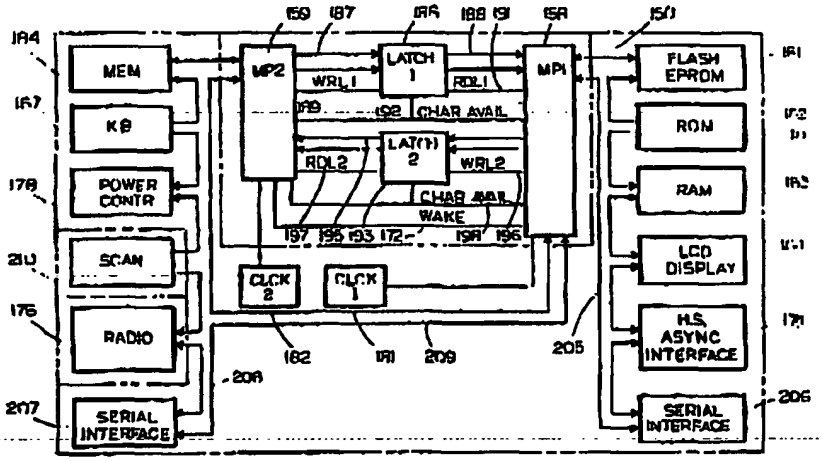
(54) Title: HAND-HELD DATA CAPTURE SYSTEM WITH INTERCHANGEABLE MODULES AND INTERACTIVE CONTROL CIRCUITS



(57) Abstract

A battery powered, portable, hand-held data terminal (10) of modular structure includes a base module (16, 136) with a keyboard (18) and a display screen (19) and their respective electrical functions (167, 164). A data and communications module may be selected from a number of different data and communications modules (48, 55, 75, 135) each having different types of data communications transceiver, or including in addition data collection devices, such as shelf label readers or bar code readers (76). The base module (16, 136) includes a microprocessor-controlled data communications and control interface having a predetermined protocol. To adapt the various type of data and communications modules for selection of any one thereof to become attached to the base module and function therewith, each of the data and communications modules includes a microprocessor (125, 144) operable to function as an emulator to interact with the microprocessor of the base module (16, 136).

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HAND-HELD DATA CAPTURE SYSTEM WITH INTERCHANGEABLE MODULES AND INTERACTIVE CONTROL CIRCUITS

Technical Field

This invention relates generally to data collection and processing systems using portable, hand-held data terminals for collecting, selectively processing and for communicating collected data to other system elements, and more particularly to control circuits which affect the operation of the data collection terminals.

Background of the Invention

Typical operations range from manually controlled processes to automated collection processes. Manually controlled collection processes may include reading data and manually keying in such read data. Typical automated processes may include scanning indicia of information with a scanner, for example a bar code reader. Data collected by such terminals may become part of the data base of the system. Real time use of data collected by the data terminals may be implemented by communication interfaces within such data terminals.

Though host computers functioning as central processing stations of such data systems may control data bases and data flow, the hand-held data terminals are key elements for operating the data systems efficiently. Current data systems using hand-held data terminals have shown a correlation between the functionality of the hand-held data terminals and the overall effectiveness of the systems.

While progress has already been made in improving efficiency and functionality of hand-held data terminals,

there is nevertheless a continued need for improving hand-held data terminals which are readily adaptable to perform various functions and communicate with a variety of communications equipment.

Summary of the Invention

According to a major aspect of this invention, one of a plurality of special purpose data and communications modules is selectively combined with a base module or unit of a hand-held data terminal unit.

According to one particular aspect of the invention, a base unit of a data terminal unit or data terminal includes a power-saving control circuit which includes first and second microprocessor elements or microprocessors. The first microprocessor which operates at a first clocking speed and consumes power at a first power level processes data. The second microprocessor which operates at a second clocking speed and consumes power at a second power level lower than the first power consumption level controls a selective operation of the first microprocessor. The first microprocessor is selectively deactivated after each data processing operation and the second microprocessor reactivates the first microprocessor on the occurrence of an event which requires data processing operations.

According to preferred features, a user interface is disposed in an upward directed surface which would typically be facing toward a person using the data terminal. The user interface typically features a keyboard adjacent a bottom end, and a liquid crystal display adjacent a top end of a substantially rectangular, elongate housing of the data terminal. The base unit provides for a data and communications module to be attached beneath the user interface and adjacent the top end of the housing.

According to another particular aspect of the invention, the data and communications module attachable to the base module includes a communications means of one

type, such as a radio using spread spectrum modulation transmissions, the data and communications module including provisions emulating data communications of a second type, the second type of communications and the respective protocol being compatible with data circuits of the base module.

According to a further aspect of the invention, the data and communications module to be attached to the base module may include provisions for data communications and a data scanner provision for collecting data.

In yet another aspect of the invention the data and communications module may include a modem and typical telephone communications coupling either in lieu of a radio communications provision or in addition thereto. The modem may be provided in the data and communications module with a data scanning device or with alternate data identification and collection provisions.

In one particular implementation including certain features of the invention, the data and communications module is contemplated to include the combination of a radio frequency communications provision and a data identification and collection provision, and an antenna of radio frequency communications provision of the data and communications module may be pivotally mounted to be pivoted to a position out of interfering relationship with the data identification and collection provision, while optimally receiving radio frequency communication.

In furtherance of efficient adaptability of data communications modules to base modules of the data terminals in accordance with the invention, it is contemplated to provide an elastic hand strap on the downward facing surface of a data terminal for retaining manual engagement with the data terminal, the hand strap being attached at one end thereof to a base module of the data terminal. A second, opposite end of the elastic strap is slidably inserted into engagement with a guide track disposed in an outer surface of the data and

communications module. The direction of insertion is in the direction of the one end of the elastic hand strap, such that an elastic tension in the hand strap retains the slidable engagement of the other elastic hand strap with the data and communications module of the data terminal. In accordance with the invention, the elastic strap is readily removed without tools by sliding the second end along the guide track in a direction against the tension of the elastic strap.

In a further embodiment according to the invention, in which a base unit includes a data and control interface for interacting with a data and communications module, an improvement in each of a plurality of data and communications modules includes a data and control interface provision including data and control signal conversion provisions for communicating data between the data and communication module and the base module in accordance with a data protocol resident within the base unit.

Various other features and advantages of the data terminal in accordance with the invention will become apparent from the following detailed description, which may be best understood when read with reference to the appended drawings.

Brief Description of the Drawings

FIG. 1 shows a frontal view of a modular data terminal and showing a frontal or upward directed face of the data terminal, as it would typically face an operator of the data terminal;

FIG. 2 is a side view of the data terminal shown in FIG. 1;

FIG. 3 is a side view of an alternate data terminal in accordance with the invention, a particular provision in accordance with certain features of the invention for engaging and disengaging a data and communications module with respect to a base module being illustrated;

FIG. 4 is a side view of an alternate data terminal

in accordance with the invention showing particular features relating to a data and communications module in combination with a base module, such features relating to the data and communications module having an RF communications provision and a data scanning provision and including further a pivotal antenna, all in accordance with the invention;

FIG. 5 is an exploded view of a pivot joint of an antenna in accordance with a particular aspect of the present invention;

FIG. 6 is a sectional view of the antenna pivot joint shown in FIG. 5;

FIG. 7 is a partial pictorial view of an upper portion of a data terminal in accordance with the invention, showing in particular a data and communications module having telephone connector plugs for interfacing the data and communications module with telephone communications lines;

FIG. 8 is a schematic diagram of functional blocks for illustrating contemplated major functional elements of a base module and a respective data and communications module of a data terminal in accordance with the invention;

FIG. 9 is a schematic diagram of functional blocks for illustrating the major functional elements shown in FIG. 8 and for illustrating the function of emulating the interface function required by an interface circuit communicating between non-compatible communications functions of the communications or data collection functions of the data and communications module and the base module;

FIG. 10 is a schematic diagram of functional blocks representing a particular embodiment of the invention showing a spread spectrum radio communication module interacting with the base module which is modified and includes a preferred power saving microprocessor circuit;

FIG. 11 is a schematic diagram of major functional

elements and their interaction of a particular embodiment of the base module including the power saving microprocessor circuit in accordance with the invention;

FIG. 12 is a schematic diagram showing typical, frequency related current characteristics of a first microprocessor element of the circuit shown in FIG. 11;

FIG. 13 is a schematic diagram showing frequency related current characteristics of a second microprocessor element of the circuit shown in FIG. 11;

FIG. 14 is a schematic block diagram showing functions allocated to each of the microprocessor elements or devices shown in FIG. 11; and

FIG. 15 is a flow diagram showing a desired functional interaction of the two microprocessor devices in FIG. 11 in accordance with the invention.

Detailed Description of the Invention

Referring now to FIGS. 1 and 2, a data collection terminal unit, also referred to herein as data terminal, is designated generally by the numeral 10. As shown in FIG. 1, a frontal face 12 of an elongate housing 14 of a base module 16 of the data terminal 10 typical faces upward and is accessible to the user of the data terminal. The upward facing portion of the module 16 houses a keyboard module 17, including an alphanumerical keyboard 18 and a display screen 19. The display screen 19 is in a preferred embodiment described herein a 4-line by 16-character Reflective Super Twist Liquid Crystal Display (LCD). Of course, other display means may be used in its stead. The keyboard 18 includes a lower, standard numerical keyboard section 21, above which is disposed an alphabetical keyboard arrangement 22. An On-Off power key 23 is preferably placed in a leftmost position of an uppermost row on an uppermost row of five keys. The outermost keys 24 in a bottom row are configured as "CLEAR" and "ENTER", while the remaining four keys in the uppermost row are preferably configured as a set of four user-defined function keys 26.

At a bottom end 30 of the housing 14, there are located two connector plugs 31 and 32 in recesses 33 and 34, respectively. Inasmuch as the connectors 31 and 32 are disposed in the recesses, adjacent end and interleaved protrusions 36 of the housing 14 extend somewhat past the connectors to protect the connectors from damage should the data terminal accidentally be dropped or set down on the bottom end 30. A preferred embodiment of the data terminal 10 is intended to withstand without damage a drop of about 1.2 meters to a solid surface, such as concrete. The preferred connector 31 is an input-output port, as may be used for such data collection as bar code reading, for example. In such instance, the connector 31 is preferred to be a 9-pin D-subminiature connector with pins interfacing to typical 5 volt scanning peripherals. The connector 32 may be used for accessing external power sources or provide of combined power and data communication. A circular miniature DIN-type connector 32 may be used in the preferred embodiment. A top end 40 of the preferred embodiment of the base module 16 typically may not include connectors. An antenna 41 shown to extend above the top end 40 is further described in reference to FIG. 2.

FIG. 2 is a side view of a data terminal 10 of FIG. 1. The base module 16 of the data terminal 10 includes an elongate upper housing portion 43 and a battery compartment 44 attached to the upper housing portion 43 adjacent the bottom end 30. In the preferred embodiment, the battery compartment 44 is assembled as a lower housing portion to the upper housing portion 43 and is equipped with a battery compartment door 46 which may be locked to seal an opening of the battery compartment 44. Adjacent the top end 40 of the data terminal 10 a data and communications module 48 is attached to the lower edge of the upper housing portion 43. The antenna 41 extends upward from the data and communications module 48 above the top end 40 of the data terminal 10. An elastic

hand strap 49 is attached to the underside of the data terminal 10. A belt clip 50 may conveniently be mounted to the hand strap 49, allowing the data terminal to be carried on a user's belt. The elastic hand strap is attached adjacent the top end of the data terminal to the underside of the data and communications module 48 and adjacent the bottom end 30 to a sloped lower surface of the battery compartment 46.

One of the features of hand-held data terminals as disclosed herein and in the PCT application PCT/US90/03282 incorporated herein by reference relates to the exchangeability of modules of different shape and varied function. The data and communications module 48 in FIG. 2 may for example include a radio module which is externally identified by the antenna 41. The radio module may be a commercially available pretuned 1-watt (UHF) frequency modulated (FM) radio transceiver module, or any similar radio module, such as a Motorola P10™ radio model, for example.

In accordance herewith it is contemplated to provide the data and communications module 48 as a module which is readily replaceable with another data and communications module. Each such module will feature a quick exchange mounting mechanism, such as is more clearly illustrated with respect to FIG. 3, and any of a number of features packaged in one of a number of compatible data and communications modules. When mounted, the module, such as the data and communications module 48 is matched in a contour continuation along a juncture 52 to the adjacent edge of the battery compartment 44 and along a longitudinal parting line 53 of the base module 16. For example, the data and communications module 48 is sized to include the described radio frequency transceiver module, as indicated by the antenna 41. Other data and communications modules may include a similar radio frequency transceiver module and may include additional memory capacity to function with the base module 16.

Various combinations of features are contemplated in accordance herewith.

FIG. 3 shows the base module 16 and substantially in a ready position to become mounted to the base module 16 is a data and communications module designated generally by the numeral 55. The data and communications module 55 is shown to represent generally a number of such data and communications modules which may be desirably incorporated into a communications system in accordance with the invention. It may be noted that the data and communications module 55 is shown in FIG. 3 as being of somewhat relatively greater depth or thickness than the data and communications module 48 described with respect to FIG. 2. The change in outer dimensions illustrates that a number of modules of various depth are adapted to match with mounting provisions to attach the respective data and communications module 55 to the base module 16.

The data and communications module 55, as a representative module featuring the attachment to the base module 16 has a plurality of laterally disposed latching hooks or latch hooks 56 which become engaged by respective latching seats or latch seats 57 disposed along the adjacent edge of the base module 16 when the module 55 is moved toward and into engagement with the adjacent edge and then toward the battery compartment 44, as shown by the arrow. Electrical communication is established via a power and communications connector 61 the pins of which engage a mating connector socket 62 within the base module 16. A set of screws 63 may be tightened through the battery compartment 44 into a set of threaded seats 64 disposed in the adjacent wall of the module 55 to securely retain the attached module as an integrated part of the data terminal 10. At the top end of the data terminal 10, a lip or extending stop edge 66 of the module 55 engages a complementarily shaped seat 67 at the top end of the base module 16 to securely interlock the data and communications module 55 with the base module 16.

It is contemplated, for example, for the module 55 to include any of a number of combinations of diverse functional elements. For example, the module 55 may include the aforementioned transceiver, though the antenna 41 may be attached externally as shown in FIG. 2 or might be provided internally, in addition to extended data memory capacity, a modem or a reader of indicia of information may be included, such as a bar code reader, or a shelf tag reader. Shelf tag systems are known in which so-called "shelf tags" contain means for programming information into small display devices which are attached to front edges of merchandise storage shelves. The devices or tags would then retain the programmed data which may be acquired by the reader in the data and communication module 55, for example. Information may be communicated between the shelf tag and the data terminal 10 by various means including radio frequency or optical transmission. Information may be communicated via optical readers in the data and communications terminal 16 as read from liquid crystals, or by other communication such as infra red optical, or low power RF data messages.

FIG. 4 shows an alternate embodiment of the data terminal 10 in which the data terminal includes a data and communications module which includes, for example, a radio frequency transceiver module 75 and a CCD scanner module which may be disposed in a lower portion of the module 75 at 76, having a scanning window at 77. Since it may be desirable to position the scanning window near a surface at which data indicia such as bar code labels may be located, as indicated at 78, the antenna which also protrudes from the top end of the data terminal 10 is found to be interfering when disposed in a normally protruding position. It is therefore contemplated to arrange the antenna 41 in a manner in which it may be pivoted from an upwardly protruding position, such as shown in phantom lines at 81 to a tilted position such as shown by the antenna 41.

In reference to FIGS. 5 and 6, there is shown a pivotal joint which experiences little signal degradation when pivoted from such upwardly extended position to the tilted position in which the scanner window may be brought into proximity of a bar code label, for example, as described. The pivotal antenna joint includes a pivot base or pivot socket 83 into a hollow cup of which fits a pivot ball 84. Both the pivot socket 83 and the pivot ball 84 are of RF dielectric to prevent radio frequency burns of a person touching the antenna when the associated radio transceiver is transmitting. The pivot socket 83 is mounted against an outer wall of the module, such as the module 48, 55 or 75 by an antenna swivel post 85. The swivel post 85 includes a spherical top against which rests a pivot washer 86. The pivot washer is in turn urged into contact with the top of the swivel post by a cupped spring washer 87, also at times referred to as Belville washer. The urging force against the spring washer 87 is provided by a doubly-threaded antenna mounting bushing 88. An external thread of the bushing 88 screws into an upper opening of the pivot ball 84 to complete the pivot joint of the antenna. The antenna 41 screws with its base into the internal threads of the mounting bushing 88. As shown in FIG. 6, a lower dielectric skirt 89 of the antenna 41 extends downward over the outer edge of the bushing, which is of metal, to prevent exposure of the bushing. It should be understood that variations in the pivot joint may be possible within the scope of the invention.

FIG. 7 shows another embodiment and further features of the invention as described herein. The elastic strap 49 may be permanently attached adjacent the bottom end of the data terminal 10 as described herein above. At an upper end, however, the elastic strap may be attached to the exchangeable data and communications modules, such as a module 90 depicted in FIG. 7. In that the modules are exchangeable and in an effort to facilitate a quick

replacement of one module for another, the hand strap is attached to the module 90 by a guide structure 91 including left and right hand spaced guide tracks 92 and 93 which receive a guide bracket 94 attached to the upper end of the hand strap 49. To attach the upper end of the hand strap 49 the elastic hand strap is stretched beyond its normal tensioned stretched length and the guide bracket 94 is inserted into an uppermost opening between the guide tracks 92 and 93. The tension of the hand strap 49 pulls the bracket 94 into the space between the guide tracks 92 and 93 in the direction of the arrow 95. The insertion of the bracket 94 securely captures the strap 49 at its upper end. To remove the hand strap at its upper point of attachment, the bracket is simply pulled out of the uppermost opening between the two spaced guide tracks 92 and 93. The embodiment of the data and communications module 90 further shows typical telephone connector jacks 97 and 98 indicating that the module contains a typical modem unit for communication over standard telephone lines. The modem unit as shown by connectors 97, 98 in the module 90 may be supplemented by memory for data storage prior to communication by the modem. In this manner the data terminal may be used in a batch process mode, data being transmitted at times and occasions convenient for telephone hook-up. Modem connections may also take on more significance in that the data terminal may be coupled to a typical cellular telephone unit which in turn can communicate via standard telephone communication networks over vast areas. In the latter mode batch transfer of data may still be desirable, though the need for substantial data storage capacity may be reduced.

FIGS. 8 and 9 illustrate a microprocessor controlled data transfer between the base module 16 and any of a number of data and communication modules which may include various data collection and data communication transceivers including complex radios such as a spread

spectrum radio or such a modem for telephone transmission of data. Though not expressly described, it is understood that the hand-held data terminal 10 as described herein and all of its circuits, including those of attached modules are powered by a battery or power source which occupies the space of the battery compartment 44 as described herein. FIG. 8 shows a block diagram of functions of the base module 16 and a typical data and communications module designated generally by the numeral 100. The base module is operative in conjunction with a typical radio frequency transceiver provided by the data and communication module 100, for example. The base module 16 includes a typical keyboard module 102 interactively coupled to a microprocessor 104. A preferred microprocessor is a 80C196KC device which is a 16-bit microcontroller 105 with on-chip masked ROM, RAM and built-in timers, ports, analog to digital converters and a serial interface 106. Thus, the microprocessor functions as a microcontroller and as an interface for communicating data and control signals to and from the base module 16. In addition to the on-chip memory capacity, an external ROM 107 and an external RAM may be provided for additional data processing and communication capacity. Display controller and driver circuits 109 may be multi-chip circuits or may be integrated into a single device to drive the described LCD screen 110. The driver circuit is controlled by the microprocessor 104 either by direct link or via a general data bus, such as data bus 111. A typical scanner interface 115 is coupled to a 9-pin connector 116, such as the referred to D-subminiature connector which may couple a laser scanner or CCD scanner to the base module 16 for data collection.

The data and communication module 100 is of particular interest in that an improved interfacing may be obtained by coupling communication between the data and communication module 100 and the base module 16 through a microprocessor 125, such as, for example an 80C51

microprocessor circuit. Typical on board ROM allows the microprocessor to be programmed to interact with a number of devices in accordance with the stored program. The microprocessor interacts with an interface circuit 126 which may be an analog or mixed analog and digital interface circuit. The program for interacting with the interface circuit 126 may also be stored within a ROM of the interface circuit 126. The interface circuit 126 is coupled to a transceiver module 128. The microprocessor 125 may also be coupled directly to a data collection interface 129 to receive data from a scanner for reading any number of different bar codes or for providing input data from other external sources. The operation of the microprocessor 125 for coupling data to the base module 16 allows various input patterns to be processed by any of specific operational protocols controlled by the microprocessor 125, such that the data input from the data collection circuit can be made the same from any of a number of devices. Also with respect to the operation of the transceiver, in that the program for operating the microprocessor 125 may include particular address codes for data retrieval and data communication via the transceiver, the data sent via a data and control bus between the microprocessors 125 and 104 can emulate a uniform data transfer protocol to the base module 16. The simplification resulting from the microprocessor 125 increases the number of communications devices that may be represented by the data communication transceiver circuit or module.

Referring now to FIG. 9, the base module 16 is shown as being coupled to a different data and communications module designated generally by the numeral 130 in which the interface circuit 126 shown in FIG. 8 has been replaced with an interface circuit 132 and the transceiver 128 in FIG. 8 has been replaced by a transceiver circuit 134. The transceiver 134 may for example be a complex radio, such as a spread spectrum radio in lieu of an FM

transceiver, as represented, for example, by the block identified at 128 in FIG. 8. However, the program function represented by the interface circuit 132 and interacting with the microprocessor 125 permits the interactive control and data stream between the base module 16 and the data and communication module 130 to be emulated to appear to the base module 16 as being the same as the simple FM transceiver module. The reference to the particular microprocessor circuit types in the base module and in the base module 16 and in the communication module 100 or 130 are given as illustrative examples and should not be considered as limiting to the scope of the invention. The data collection interface 129 is considered optional and may not form part of the communication modules 100 or 130 when the communication module does not include a scanner module, such as indicated at 76 in FIG. 4. In either case the microprocessors 104 and 125 interact, each controlling the environment of its respective submodule, such as the base module 16 or the data and communication module 130, to enhance data exchange between the modules.

FIG. 10 shows a communication module 135 communicatively coupled to a base module 136. The base module 136 may be structurally similar or identical to the described base module 16, the electrical control functions and circuits include certain power saving functions and circuits as further described with respect to FIGS. 10 through 15. The communication module 135 is a preferred spread spectrum radio module. Spread spectrum radio transmission and receiver functions are shown with a symbolic antenna 137 as a single transceiver 138 ("SS RADIO"). Spread spectrum radio technology is well known in the art as permitting high binary data rate transmissions which are propagated over a selected channel frequency within an assigned 902 to 928 Mhz commercial frequency band. Spread spectrum communication may use a pseudo-noise encoding mechanism according to which data

are encoded, transmitted, received and decoded at respective transmitting and receiving stations. Both the transmitting and the receiving station must of course employ identical encoding and decoding algorithms. The encoding and decoding function is shown as a spread spectrum radio modem circuit 139 ("SST"), an integrated circuit device which might well be considered an integral element of the spread spectrum radio unit. Spread spectrum radio transmissions are capable of encoding, decoding and transmitting binary data messages at relatively high rates in comparison to other data transmission rates. While state of the art facsimile transmissions and typical FM radio transmissions may take place at signalling rates of 9600 baud or bits per second, in a preferred embodiment a spread spectrum binary transmission rate is 192 thousand bits per second. A transmitted message includes of course besides data bits various control and error checking bits. Outgoing messages are modulated and incoming messages are demodulated by the modem circuit 139 and are communicated as synchronous demodulated serial messages between the modem circuit 139 and a high level serial communication controller 141 ("HSCC"). A timing function circuit 142 ("TIMER") is shown as being coupled to the communication controller 141. It is to be understood, however, that the timer 142 is also functionally coupled to the circuit 139 and further provides timing signals to operate a radio module microprocessor circuit 144 ("PROC CRCT.") and an associated external memory circuit 145 ("DAT MEM").

The serial communication controller 141 performs control functions on data messages, such as error detection and correction, and converts data messages from synchronous serial to parallel binary data. The controller operates under a known communication protocol referred to a High level Data Link Control or HDLC. Data are communicated between the serial communication controller 141 and the microprocessor circuit 144 in a

synchronous parallel data format. The microprocessor circuit 144 receives and temporarily stores received data in a typical memory circuit represented by memory circuit 145. Data are then communicated by the microprocessor 144 as high speed asynchronous data communication messages between the communication module 135 and the base module 136. The microprocessor 144 is preferably an H8 type microprocessor which includes on-board memory in the form of both ROM and RAM circuits. The on-board memory stores the communication control instructions by which the microprocessor 144 communicates with the respective data circuits in the base module 136. However, to adequately support temporary storage of data messages to relay them as either synchronous or asynchronous communication messages between the modules 135 and 136, the memory circuit 145 externally of and in addition to the on-board memory is available to the microprocessor 144.

The circuit functions in the base module 136 of FIG. 10 depict a power-conserving microprocessor control circuit 150 which includes a combination of two microprocessor elements 158 and 159. The microprocessor elements 158 and 159, individually capable of functioning independently of each other are coupled to interact as a functional control unit to conserve power when compared with a conventional microprocessor controlled circuit. The microprocessor 158 which is referred to as application processor 158 is applied to perform data processing and data manipulation operations of the data terminal 10. The second microprocessor 159 is referred to as a control processor 159. The application processor 158 operates faster than the control processor 159 but also consumes more power. However, to conserve power in the combined operation of the two processor elements 158 and 159, the application processor becomes deactivated after completion of any data processing task. Since data storage and screen display of data are memory intensive functions of the application processor 158, the processor 158 is

coupled to a full complement of memory including programmable read only memory 161 ("FLASH EPROM"), permanent memory 162 and random access memory 163 ("PSRAM"). Though the application processor 158 updates a screen display 164 ("LCD DISPLAY"), the control processor 159 controls a contrast adjustment 166 ("CONTRAST LCD DISPLAY"), the commands for which may be received from an operator through a keyboard 167 ("KB"). Data and control characters are communicated between the application and control processors 158 and 159 via an interface circuit 168 ("INTRFACE CRCT"). The interface circuit may be an integrated circuit which further includes functions for applying respective clocking signals from a clocking signal source 169 ("CLK1") to the microprocessors 158 and 159. The interface circuit also may include functions such as the control of an EL panel backlight drive 171 ("BCKLIGHT DRIVE").

Since the application processor 158 becomes deactivated upon completion of a data processing task, the control processor 159 functions to reactivate the application processor 158 upon occurrence of an event that necessitates data processing or manipulation. Such activation is preferably provided by a direct connection between the two processors 158 and 159 as shown at 172. High speed data transfer between the communication module 135 and the base module 136 of the data terminal 10 are preferred to take place directly between the microprocessor 144 of the communication module 135 and the application processor 158 via a high speed asynchronous communication interface circuit 174 ("HS ASYNC INTR FACE"). In a preferred data receiving operation the microprocessor 144 would prompt the control processor 159 to reactivate the application processor 158 to receive incoming data through the interface circuit 174. Reactivation of the application processor 158 for an outgoing message may be prompted by an operator from the keyboard 167.

Referring to FIG. 11, the schematic diagram shows major functional logic and communications elements of the power-conserving microprocessor circuit 150 which may be controlling the operations of, or be functional in the operation of, the hand-held, portable data terminal 10, schematically identified by encompassing box. The data terminal 10 may interact in particular with one or more temporarily attached or integrated peripheral communication devices or modules, such as a transceiver communication module ("RADIO"), shown at 176. The communication module may be a standard FM transceiver adapted for digital data communication, or it may be the spread spectrum communication module 135 described with respect to FIG. 10. The data terminal 10 of the described example being portable, the physical circuits of the functional devices shown in FIG. 11 typically would be powered by a battery 177 (shown schematically in FIG. 14) which is included in the power management function 178 ("POWER CONTR"). The microprocessor operated control circuit 150 comprises, as referred to with respect to FIG. 10, a combination of two circuit portions which include specifically the two microprocessor type subcircuits 158 and 159. Each of these subcircuits 158 or 159 are separately functioning microprocessor blocks, modules or separate microprocessor devices. In reference to FIG. 11 the devices are respectively the application processor 158 ("MP1") and the control processor 159 ("MP2"). It is advantageous to perform data processing operations at a comparatively high speed and with a more powerful processor than would be desirable for relatively less complex control functions.

The term "data processing operation" is used herein in the sense of manipulating a series of binary codes according to programmed instructions to arrive at a desired result. Because of the great number of discrete binary operations required to perform many of the most common data processing functions, higher processor speeds

and more complex or powerful microprocessor circuits of those typically available are more desirable for data processing operations.

A characteristic of more powerful microprocessor devices and those operating at higher speeds is that these devices also consume more power. However, in accordance herewith, the power consumption of a microprocessor circuit may be limited as further described. For example, in the preferred embodiment, the application processor or data processing processor device 158 is an "Intel 80C188EB" device which is "16-Bit" microprocessor device, operated at a preferred speed of 9.2 megahertz (MHz). At such preferred clocking speed of 9.2 MHz, the power consumption or operating current consumed by the data processing microprocessor device 158 is approximately 55 milliamps ("mA"). The control processor 159 is in a preferred implementation a "Hitachi H8/325" device which is an "8-Bit" microprocessor, operated at a preferred speed of one-half of the speed of the data processing microprocessor 158, or 4.6 MHz. Because of the smaller physical size of the control processor 159 and the slower, preferred clocking speed, the power consumption or current required by the control processor 159 in its operational mode is only about 9 mA, hence less than one-fifth of the power consumed by the processor 158. Because of continuous advances in the field of microprocessors over the past decade, it is to be expected that in the future other microprocessors will be marketed which will meet or exceed the requirements of the presently preferred microprocessors and that these microprocessors also may operate in accordance herewith. In general, the control microprocessor circuit or the control microprocessor 159 desirably operates at a slower and less power consuming speed than the application microprocessor circuit or the application microprocessor 158. A one-to-two speed ratio for driving the respective microprocessors 159 and 158 is preferably chosen because of the power savings that are

being realized with respect to the portable data terminal 10. Respective clocking circuits 181 and 182 ("CLCK 1 and CLCK 2") are shown as providing respective timing signal ports coupled to the respective processors 158 and 159 to drive the processors at the desired speeds as described.

Also, a functional arrangement of the separate clocking circuits 181 and 182 preferably may be replaced by the single crystal oscillator circuit 169 ("CLK 1") which is then coupled through the interface circuit 168 ("INTERFACE CRCT") to both processors 158 and 159 as shown in FIG. 14. The interface circuit 168 would include in such coupling arrangement a typical divide-by-two timing circuit function. An original 9.2 MHz clocking signal port and a signal port with the divided by two signal, comparable to the clocks or timing signal ports 181 and 182, would be coupled to the respective timing signal input ports of the processors 158 and 159, respectively, to drive the processors 158 and 159 at their respective speeds of 9.2 and 4.6 MHz. A second clock 183 ("CLK 2") shown in FIG. 14 may provide what is referred to as "real time" timing functions such as actual time and date information.

As will become apparent from the further description, it is within the scope of the invention to integrate the distinct functions and operational characteristics of the separately identified microprocessor devices 158 and 159 into a single integrated device. The resulting integrated device 150 desirably includes respective interface functions as are further described herein to implement the power-saving characteristics realized by the presently preferred embodiment of the control circuit 150. Within such integrated device 150, the function of the application processor 158 is then performed by a first microprocessor circuit block or circuit portion, and the function of the control processor 159 is performed by a second microprocessor circuit block or circuit portion. These circuit blocks, portions or modules interact

essentially in the same manner within the circuit 150 as the currently used microprocessor devices 158 and 159.

The preferred control processor 159 includes in its commercial implementation in addition to typical microprocessor registers and an arithmetic logic unit such functional circuit blocks as ROM, RAM and communications ports. These circuit blocks may also be included in any integrated device 150, or their functions may be supplied by peripheral devices. As shown in FIG. 11, additional external memory 184 ("MEM") may optionally be provided to supplement such on-board memory 185 ("OM"), though for typical operations as further described herein, the external memory device 184 is not required. According to a preferred embodiment, data communication between the processors 158 and 159 occurs via an interface circuit including, for example, two 8-bit data registers or latches described in greater detail with respect to the further description relating to FIG. 11. It is to be understood, however, that the control processor 159 may have a direct bus interface provision and become directly coupled to the application processor 158, the coupled processors 158 and 159 thereby being capable of bidirectionally passing data and control signals without the described two 8-bit data registers or latches. The interface circuit 168 shown in FIG. 14 should be understood to not only include the clocking signal coupling circuits to drive the respective application processor 158 and the control processor 159, but to further include the data interface or bus to permit the desired bidirectional data and control code communication between the processors 158 and 159 as further described herein. In further reference to FIG. 14, an integration of the processor devices 158 and 159 into a single device desirably may include the interface circuit 168 as an integral part of the integrated circuit 150.

Referring again to FIG. 11, a first latch 186 ("LATCH 1") of the two latches is coupled through an 8-line

parallel bus 187 to the microprocessor 159 and through a similar bus 188 to the microprocessor 158. Respective write and read lines 189 and 191 ("WRL1 and RDL2") provide respective control or trigger signals for the processor 159 to write data into the first latch 186 and for the processor 158 to read data from the latch 186. A handshake or control signal line 192 ("CHAR AVAIL 1") toggles between a high or "logical 1" to indicate to the processor 158 that data have been read into the first latch 186 by the processor 159 and a "logic 0" to signal that the processor has read or taken the data from the first latch 186. A second latch 193 ("LATCH 2") similarly stores an 8-bit data element written into the second latch 193 by the processor 158 over a second write 8-bit write bus 194. A second read bus 195 transfers the data element stored in the second latch 193 from the latch to the second processor 159. The control or trigger signals for writing into or reading from the second data latch 193 are provided over trigger lines 196 and 197 ("WRL2 and RDL2"), respectively. A second handshake or control signal line 198 ("CHAR AVAIL 2") coupled to the second latch 193 and to the processors 158 and 159 also toggles between high and low signal states to indicate in the high state the availability of data in the second latch 193 and in the low state the completion of a read operation of the most recent data element by the control processor 159.

The control signal line 172, referred to with respect to FIG. 10, carries a control signal generated by the control processor 159, by which the control processor 159 controls the duty cycle of the application processor 158. In reference to FIGS. 12 and 13, the current usage and respective power consumption of the control processor 159 ranges between a typical operating mode and a typical "idle mode" at the preferred frequency of 4.6 MHz between a high of 9 and a low of about 7 mA, as shown in FIG. 12 by graphs 201 and 202, respectively. It should be realized that even while considered "idle", the control

processor maintains power to internal memory and performs typical periodic monitoring functions, such as strobing the keyboard circuit 167 ("KB") for a "Depressed Key" signal, for example, or routinely monitoring the power management function 178, such as for a "Low Battery" indication. However, even when in the typical operational mode as indicated on the current vs. frequency graph 201, the control processor uses only about one-sixth of the current used by the application processor 158 in its preferred operational mode. On the other hand, when the application processor 158 is placed into an idle state in which the device 158 is not driven by a clocking signal, the idle state current requirement has a specified maximum rating of 0.1 mA, as shown by the high-low indicated values at the 9.2 MHz frequency mark at and below graph 203 in FIG. 13, in which graph 203 indicates the typical operating current consumption of the application processor 158. It is to be noted that a deactivation of the application processor 158 could be implemented by a complete electrical shut down of the device. However, because of the low non-clocked power or current draw of the application processor 158, the application processor function is preferably deactivated by eliminating its clocking signal but maintaining the device 158 under DC bias. Removing the clocking signal from the application processor function achieves a desired power-down idle state while permitting the device 158 to be reactivated momentarily by an appropriate "wake up" control signal from the control microprocessor 159.

Tests have shown that typical data processing operations performed by the application processor 158 require approximately 10 milliseconds of time and not more than 20 milliseconds on the average of all operations which are typically performed by the application processor 158. It has further been found that a more user friendly and a more practical response time may be obtained from the data terminal 10 and less power is required when

substantially all data processing operations are performed by the application processor 158 and the application processor is subsequently immediately deactivated, than if a single alternative microprocessor circuit were used which would operate at a higher rate and would include sufficient computing capacity to perform all required functions in good time. The combination of the application processor 158 and the control processor 159 amount in the preferred selection of the two processors only to an approximate increase in current usage of typically about ten percent and in the extreme of no more than 20 percent over the normal operating current level of the control processor by itself. An upper combined power consumption of the application processor 158 as controlled by the control processor 159 and the control processor 159 itself is about one fifth of the power consumption of the application processor when it is operated continuously. However, the display speed and data manipulation speed of the data terminal 10 essentially is the same as if the data terminal were controlled by the more powerful application processor 158.

The operating current requirement for the application processor 158 is related to the increased number of actively switching elements in each computational operation. Though having an interrupt function, the preferred 80C188EB processor 158 does not include, in contrast to the control processor 159, any internal memory devices. FIG. 11 consequently shows a data bus 205 of the processor 158 coupled to external memory devices, such as a flash electrically erasable and programmable read-only memory 161 ("FLASH EPROM"), a read-only memory 162 ("ROM") and a typical random access memory 163 ("RAM"). The data bus 205 further couples the application processor directly to the data display 164 ("LCD DISPLAY") of the data terminal 10, such as a dot addressable LCD graphic screen, for example. A direct data transfer by the high speed application processor 158 to the LCD screen is preferred

because of substantial amounts of data handling or processing that is required in updating a particular screen. For example, even a small graphic screen display, such as a preferred screen of 48X100 pixels, requires that each of the pixels be updated on a continuous basis. Typically control circuits, which are typically part of the data display function 164 and are not separately shown, and which may be specific to a particular screen display may routinely re-apply currently displayed information dots in a cyclic refresh operation to the already identified pixels of the screen. However, in any updating of the screen, such as a simple display line scrolling operation, which an operator may not even consider noticeable or significant, each pixel of the screen must be updated. To perform such updating of information in a power efficient manner, a data processing operation and the high speed passing of the updated data between the RAM memory 58 and the data display 164 is most power-economically and most promptly and, hence, most user-friendly performed by a short operational activation of the application processor 158. More data processing with respect to the data display screen 164 may be required for routine menu operations. Menu operations are particularly desirable for such portable data terminals 10, in that the typical user would not be expected to be well acquainted with computer terminals. Well defined menu operations with a number of available menu levels are found to significantly increase the usefulness of a data terminal unit. An efficient menu operation is known to involve data base searching and data retrieval in addition to the normal display screen updating operation. In the above-described operations the described microprocessor circuit with the selectively activated data processing device 158 and the relatively smaller and slower control processor 159 has been found to be particularly advantageous.

A selective activation and deactivation of the

microprocessor circuit portion implemented by the data processing device or application processor 158 would also provide for power savings when the operating speeds of the two processors 158 and 159 are the same. Though in the event of both processors 158 and 159 being operated at the same speed, the power savings do not appear to be as prevalent as realized in accordance with the preferred embodiment of the described invention.

A further function to be advantageously addressed by the application processor 158 is the data communication with the high speed asynchronous communication interface 174 ("H.S. ASYNC INTRFCE"), in support of facsimile or external display screen operations. Of less significance, yet typically power saving, are data communications to an RS-232/RS-485 serial interface 206 ("SERIAL INTERFACE"). However, it should be realized that certain communications operations, such as outgoing communications to a printer (not shown) for example, may also be communicated under the control of the control processor 159. Even when the application processor 158 selects data for communication to a line printer, a typical printer speed, except in a graphics mode would be sufficiently slow to allow the application processor 158 to operate in an intermittent, power saving mode. FIG. 11 consequently shows a second RS-232/RS-485 interface 207 ("SERIAL INTRFCE") coupled to a second data bus 208 which is further communicatively coupled to the control processor 159 to support the above described data communication operation via the control processor 159.

The data bus 208 is further shown as being coupled through a bus extension 209 directly to the application processor 158. The data bus extension 209 is particularly provided for direct data communication between the application processor and a data scanner 210 ("SCAN"), which may for example be a bar code reader. Because of the high rate at which data are generated by the operation of a data scanner, the data are most reliably received,

processed and stored by the application processor, though the operation may not be power saving as such. A scanning operation may consequently involve the operation of both the application processor 158 and the control processor 159. According to a preferred operation of the control circuit 150, the control processor 159 monitors the circuit function of the data scanner 210 to detect a control signal which indicates the event of a scanner trigger depression and that a scanning operation of an associated physical scanning device is about to begin. The scanning operation results in a string of data appearing at the data bus 208 and the associated data bus 209. Since the application processor 158 is likely to be idle at the time of the occurrence of a trigger signal, the control processor places a "wake-up" signal on the control signal line 172 to activate the application processor 158. The control processor 159 further writes an 8-bit control character into the first latch 186. Upon completion of loading the control character into the data latch 186, the control processor 159 places a "one" signal on the character available line 192 to allow the application processor to read the control character from the latch 186. The application processor reads and decodes the control character in accordance with protocol instructions read from the ROM memory 162, for example. In the example of a scanner trigger indication, the decoded control character would signal the forthcoming string of information to be received by the application processor 158 directly from the scanner 210 over the data bus 209. Hence in contrast to being conditioned for the event of receiving data from the keyboard 167 or from the radio 176 which data might preferably be received over the data latch 186, the application processor would in the event of scanned incoming data be conditioned to read the "event data" as a string of data directly from the data bus 209. The term "event data" is used to describe data relating to an event. Any time event data requires

processing, such event data would be routed to the application processor 158 either directly as described with respect to the scanner data or between the two processors 158 and 159, such as by the interface 168, for example. It is to be understood that conditioning the application processor to receive a string of data directly via the bus 209 need not be limited to the receipt of the scanner data but is contemplated with respect to any such future uses of the data terminal 10 which requires any high volume of data to be received and processed within a, comparatively to other typical serial receipt of data, brief period of time. Upon completion of the scanning operation, a trigger release signal would be loaded into the first latch and communicated from the control processor 159 to the application processor 158. Upon receipt of the signal and completion of any data processing operations remaining as a result of the receipt of data via the data bus 209, the application processor instructs the control processor to apply a "wake-up" signal to the control signal line 172 upon occurrence of any specified event requiring processing of data, after which the application processor re-enters an idle state. Thus, in accordance with the presently preferred embodiment, in the event of the direct receipt of a string of data by the application processor 158, the control processor 159 continues to control the application processor 158 in transmitting control codes to selectively enable or disable the application processor 158 to directly receive data via the data bus 209. The receipt data by the application processor 158 is referred to as "direct" data input, since the contemplated transfer of data via the data latches 186 and 193 or via the interface circuit 168 is bypassed.

FIG. 14 shows in form of a block diagram preferred electrical components of an exemplary data terminal 10, and of the preferred interactive relationship of such components to the application processor 158 or the control

processor 159. FIG. 14 shows schematically a plurality of electrical components which are generally directly related to the functional elements discussed with respect to FIG. 11. In the embodiment shown in FIG. 14, the application processor 158 controls directly the previously referred to high speed asynchronous communications interface 174 and the RS-232/485 standards serial interface 206. The flash EPROM programmable read-only memory 161 is in the embodiment of FIG. 14 identified as having a preferred 256K byte storage capacity. The flash EPROM supplements the standard ROM memory 162 which is preferred to have a 512K byte storage capacity. In the preferred example of the data terminal 10, the ROM provides the typical and normally non-variable data processing protocol instructions and includes control instructions for standard display updating routines as well as other routines which are typically implemented by standard keyboard instructions and which pertain to typical data input and output commands.

The random access memory 163 is in the specific embodiment a semi-permanent static RAM type circuit and has a preferred capacity of 512K bytes. The preferred data storage capacity has been determined to provide sufficient storage for an on-board data base related to typical inventory or delivery route type information. In view of the portability of the data terminal 10, an unexpected loss of battery power may bring about a significant loss of information unless the data stored at the time of a temporary loss of battery power are protected from destruction until full battery power is restored. For example, the data terminal 10 may be returned at an initial signal of "low battery" to a battery charger unit (not shown) for a recharging operation and any stored data may be transferred, even while the battery 177 is being recharged, from the data terminal 10 to a host computer (not shown).

A preferred LCD display 164 is a graphic display

having an array of 48 x 100 pixels. Typical menu or special graphic screen data may be pre-established for a particular data terminal 10 or for an application group of such units and may be stored initially in the specific ROM 162 provided for the particular unit or units 10. As previously discussed, the updating of displayed data on the screen device 164 requires a significant amount of data processing. Typically, such data processing operations involve accessing permanently stored screen display information, such as from the ROM 162 or from the flash EPROM 161, the manipulation of such information, and temporary storage of such manipulated information in the random access memory 163. As shown in FIG. 14, the application processor 158 has direct functional control over the respective devices for such data updating manipulations with respect to the LCD Display screen 164.

Another function related to the preferred LCD display screen 164 involves a contrast control circuit 166. The contrast of the LCD display screen 164 is typically set and adjusted by an operator and is a matter of choice. The contrast may be adjusted for example by a typical key depression or by a keyboard sequence given by an operator. Such control input executions are within the scope of operations of the control processor 159. Thus, in response to an appropriate command from the keyboard 167, the display contrast may be changed without activating the application processor 158. The contrast display may be controlled as indicated in FIG. 14 by the functional coupling of the keyboard circuit 167 to the control processor 158 and the further coupling of the processor 158 to the contrast control circuit 166 and then directly to the LCD display screen circuit 164.

The LCD display screen 164 in the preferred embodiment is equipped with a backlighting drive. Many warehouse operations, route delivery operations and even merchandising inventory operations require at least some operations of the data terminal units to be performed

under sufficiently poor lighting conditions to suggest a need for a backlighting source to be supplied as a standard feature of the LCD display screen 164. The backlight drive circuit 171 is preferably coupled through the interface circuit 168 to the control processor 159. In that such a backlighting circuit may have a need for adjusting, for example, the brightness or luminescence of the circuit, both the application processor 158 and the control processor 159 may interact through the interface circuit 168 to provide for an operator controlled brightness control sequence to be communicated to the backlight drive 171.

It should be realized that the interface circuit 168 is a simplified schematic representation of a large-scale integrated circuit 168 which includes timing function circuits for the real time clock and its functions, as well as for providing the clocking signals to each of the two processors 158 and 159. The circuit 168 further provides the already described data communication functions between the application processor 158 and the control processor 159 as represented in FIG. 11 by the two latching circuits 186 and 193. The function by the control processor 159 to activate or "wake up" the application processor for data processing operations is accentuated in the representation of the "wake-up" feature by the separate function line 172 in FIG. 14. In one contemplated embodiment the interface circuit 168 may include integrally a switching circuit function for separately switching the application processor 158 off or on, as indicated by the function blocks "#1 OFF WAIT" and "#1 ON", as shown in FIG. 15. Such a switching operation may be implemented by a typical switch as part of the integrated interface circuit 168 which selectively interrupts and reestablishes the clocking signal to the application processor 158. The function of deactivating and reactivating the application processor is controlled in a preferred embodiment via the interface circuit 168 in

a somewhat different manner. Instead of controlling the clocking circuit to the application processor 158 in the integrated circuit with a control signal from the control processor 159, the control function is preferably split. It has namely been found expedient for the application processor 158 to provide a shutdown status signal to the control processor 159 and to shut itself down. The control processor 159 subsequently returns the application processor 158 to an active state upon occurrence of any event which requires the operation of the application processor 158. The process flow diagram of FIG. 15 generally depicts operational procedures between the application processor 158 and the control processor 159.

Further in reference to FIG. 14, a trigger control signal of the scanner 210 is preferably received by the control processor 159. However the data flow from the scanner 210 will be received directly by the application processor 158 for further processing and storage. Input signals which are received at speeds within the operational envelope of the control processor 159 are received by and transferred through the control processor 159. For example, key depression signals from the keyboard 167 are preferably received directly by the control processor 159. A preferred keyboard size for the data terminal 10 referenced herein, as indicated in FIG. 14 is a 6x8 key matrix. Such a choice is made based on space considerations and requires that multiple functions may be implemented by each of the keys. However, the selection of a preferred keyboard remains in any case one of choice and has no particular bearing on the gist of the invention. Because of the "slow" realtime selection by an operator in comparison to the "fast" processing speed of even the slower control processor, the selection interpretation of which key function has been selected by an operator may be made by the control processor 159. An "event" indication character communicated to the application processor 158 preferably reflects already

which of the available functions of a particular key has been selected. The preprocessing of relatively slowly occurring events has been found to advantageously limit the operational periods of the application processor 158.

The control processor further controls an input to an audible alarm circuit 211 ("BUZZER"). An audible alarm is a slowly occurring input signal to generate a signal at audio frequency, so as to alert an operator of an alarm condition or to signal that a processing operation has been completed. For example, when the application processor 158 has received a string of data from the scanner 210, and has further processed the received information to verify its correctness, the application processor 158 may communicate an acceptance code to the control processor 159 and be shut down from further operation. The control processor will then routinely generate an audible signal to alert the operator of the unit of the acceptance of the code read via the scanner, for example. Prior to communicating the acceptance code to the control processor, the application processor may have retrieved from its memory 163, for example, information relating to the bar code which has just been read and accepted, and may have compiled an information screen displaying such retrieved information to the operator prior to the deactivation of the application processor 158. Thus, by the time the operator is alerted by the audible signal that the respective bar code has been read and accepted, the pertinent information regarding the item represented by the bar code is already displayed on the LCD display screen 164.

Other devices which are preferably under direct control of the control processor 159 are the radio 176 with its included radio interface ("RADIO INTERFACE"), and the power control circuit 178 ("CHARGE/ POWER CONTROL") of the data terminal 10. The serial interface 207 ("RS-232/RS-485 SERIAL INTERFACE") may optionally be controlled by the control processor 159. Based on the power saving

interaction between the application processor 158 and the control processor 159 various other additions of devices or functions to the general operation of the data terminal 10 may be feasible without unduly limiting the operational cycle of the data terminal 10.

The interaction between the control processor 159 and the application processor 158 is described in greater detail in reference to both FIGS. 14 and 15. In general, the operations of the application processor are restricted to data processing operations while the operations of the control processor 159 pertain to input-output control functions which include periodic monitoring functions, such as monitoring the state of the battery 177 via the charge/power control circuit 178. Though being less powerful and operating slower than the application processor 158, the control processor 159 controls the activation or reactivation of the application processor 158. However, the application processor 158 is preferred to process the parameters and feed the respective instructions to the control processor 159 by which the control processor is operated. The application processor 158 is therefore according to the preferred embodiment the one device which accesses the operations protocol of the data terminal 10 from either the ROM 162 or the flash EPROM device 161.

With the depression of the power switch by an operator, the data terminal unit is physically started with a cold start ("POWER ON"). The turn-on starts the clocking signal and the reset of both the control and application processors 158 and 159. The control processor 159 may reset the application processor 158 ("RESET #1"). The reset operation starts the apparatus ("START APPARATUS") with an initialization sequence of communications between the application processor 158 and the control processor 159. During the initialization the application processor 158 retrieves from its program storage default values, such as for a battery threshold

value and transfers the respective default value to the control processor 158 ("COMM.1"). The control processor retains the default value and uses it in its further operations to operate the power control circuit 178. Other initialization values may be communicated to set an initial contrast value on the LCD screen display 164 ("COMM.2"), and whether or not the backlighting function is to be turned ("COMM.3"), for example. The application processor 158 further may retrieve data from memory 161, 162 or 163, and manipulate such data to place an initial screen display on the screen to signal to the operator that the data terminal 10 is operational. Upon completion of data manipulation and communication of the default values for initializing the data terminal 10, the application processor 158 communicates to the control processor 159 that it is assuming its rest state ("#1 OFF WAIT") and is shut off pending the occurrence of an event.

Upon occurrence of an event, such as a "battery low indication" or the depression of a key by the operator of the data terminal 10, the control processor 159 causes the application processor 158 to become turned on ("#1 ON"). Typically the clock signal to the application processor 158 may be provided by a control signal applied to the interface circuit 168, or the application processor may become otherwise enabled, such as by an enable signal applied to the control signal line 172. Upon having become activated, the application processor 158 communicates with the control processor 159, such as via the interface circuit 168 in the manner also described with respect to FIG. 11, to request ("#1 REQU. EVENT") data as to the type of event that has occurred. After receiving the respective communication from the control processor 159, the application processor 158 tests the received information as to the type of event and proceeds to process data as required according to the program. FIG. 15 shows three typical events of a large number of programmed events for which the application processor 158

may be activated. A typical key depression may result in reading the value of the depressed key from the second data latch 193 as described with respect to FIG. 11, or from an equivalent register of the integrated circuit 168 in FIG. 14. The information then results in the retrieval of data regarding the addresses of pixels which will be changed to a logical "high" to depict the information on the LCD display screen 164, the respective data being transferred to the respective circuit elements of the display screen 164. Thereafter, the application processor communicates to the control processor 159 that the instructions have been executed and is shut down to await a further activation and "EVENT" instruction. The shutdown of the application processor 158 may be initiated either by the application processor 158 itself or by the control processor 159. Because the start-up or activation of the application processor 158 is initiated by the control processor 159, it may be desirable to disable the application processor 158 through the control processor 159.

Another typical event for activating the application processor 158 may be the detection of a low battery indication in response to a threshold value transferred by the application processor 158 to the control processor 159 during the described start-up procedure. The protocol may require that the application processor 158 verify the low battery indication by providing its own comparison check. Because of an impending shutdown due to a low battery indication, the application processor may complete any operation if the low battery indication is still within tolerable low limits or may suspend further data processing because of risk of errors in its operation due to the low battery voltage. The application processor may further display a low battery indication ("DISPLAY LOW BATT WARNING") on the LCD display screen 164 and then be shut off pending further event instruction as shown in FIG. 15.

Another type event may be a special function key instruction such as the indication that a menu operation has been selected. The application processor 158 proceeds to access a designated program routine corresponding to the requested menu choice ("RETRIEVE MENU DATA"). The respective program instructions are executed ("PROCESS DATA"), and the result or completion of the routine is displayed on the LCD display screen 164 ("DISPLAY DATA"). The displayed result may be preceded by a repetitive interactive data transfer between the application processor 158 and the control processor 159, for example, when the menu choice requires the transmission of displayed information to a host computer. In such an event the application processor 158 may transfer the displayed information character by character to the control processor 159. The control processor 159 in turn activates the radio interface and transfers the information string to the radio interface to be transmitted in accordance with the program instructions interpreted by the application processor 158. FIG. 15 shows an error trap ("ERROR") to which the program instructions proceed if an event code is not recognized by however many event descriptions and resulting processing routines by the application processor 158 may have been programmed into the application program for the particular application of the data terminal 10. It has been found that on the average, data processing operations performed by the application processor 158 require less than 10 milliseconds. Thus, on the average, operations including the processing of keystrokes and the associated display manipulations require less than one fiftieth of the average operational period of the data terminal 10. Substantial power savings are consequently achieved by selectively de-activating and re-activating the application processor for preprogrammed events which require the execution of the respective data manipulations at a speed which is not obtainable by the preferred

control processor 159.

Further in reference to FIG. 15, if none of the event tests recognize the particular code supplied for identification to the application processor 158, an event error trap routine ("ERROR") would be used to inform the operator of the error condition. Such a routine may, for example, instruct the operator to again enter the most recently requested operation, and may accompany the error routine by an audible warning from the buzzer. Various changes in the described preferred control sequence may be implemented. Certain routines may be implemented at the described slower speed by the control processor 159 directly, while the application processor 158 remains deactivated. Other changes may be made in the selection of the first and second microprocessor devices 158 and 159 as application and control processors, respectively. The described microprocessor devices have been found particularly suitable for various operations that were expected to be performed by the data terminal 10 in the above-referred to operations.

Various changes and modifications in the structure of the described embodiment are possible without departing from the spirit and scope of the invention as set forth in the claims.

CLAIMS:

1. A hand-held data collection terminal unit comprising:

a base module including a keyboard, a display, means for storing a control program and data, an interface for communicating data and a microprocessor for controlling data applied to and received from said interface in accordance with such program; and

a data and communications module including a selected one of a plurality of data communication transceivers each having unique transceiver operation signal patterns, the data and communications module further comprising a communications interface and a microprocessor communicatively coupled to the communications interface of the data and communications module and coupled to the microprocessor of the base module, the microprocessor of the data and communications module controlled to communicate data to the microprocessor of the base module in accordance with the program of the microprocessor of the base module.

2. The hand-held data collection terminal unit according to claim 1, wherein the data and communications module further comprises a data collection means having a data transfer link coupled to the microprocessor of the data and communications module for controlling the data communications between said data collection means and the base unit in accordance with the program of the microprocessor of the base module.

3. The hand-held data collection terminal unit according to claim 1, wherein the data and communications module further comprises a code reader, the code reader having a data transfer link coupled to be controlled by the microprocessor of the data and communications module for transferring data between the data and communications module and the base module in accordance with the program of the microprocessor of the base module.

4. The hand-held data collection terminal unit

according to claim 3, wherein the code reader is a CCD bar code scanner, wherein the selected communications transceiver is a radio frequency transceiver, the data and communications module having an antenna extending away from the data and communications module and the data collection terminal, the antenna being pivotally mounted to pivot away from a scanning direction of the CCD bar code scanner permitting the CCD bar code scanner to become in proximity of a bar code label to be read.

5. The hand-held data collection terminal according to claim 1, wherein the data and communications module is attached to the base module by a plurality of engaging latch hooks and corresponding latch seats and means for maintaining the engaging position.

6. A microprocessor circuit for use in data processing apparatus comprising:

means, including a first microprocessor circuit portion and signal input means for driving the first microprocessor circuit at a first clocking speed, for performing data processing operations on data signals at the first clocking speed;

means including a second microprocessor circuit portion and second timing means for driving the second microprocessor circuit portion at a second clocking speed for controlling input and output signals to and from the microprocessor control circuit;

means for communicatively coupling the first and second microprocessor circuit portions to each other to bidirectionally pass data and control signals there between; and

means for selectively deactivating the first microprocessor circuit portion upon the first microprocessor circuit portion completing a data processing operation, and for selectively reactivating the first microprocessor device in response to a control signal from the second microprocessor circuit portion, whereby the first microprocessor circuit portion remains

deactivated during periods during which no data signals are processed.

7. The microprocessor circuit according to claim 6, wherein the data processing means, the input and output controlling means and the coupling means are supported on a single circuit device.

8. The microprocessor circuit according to claim 7, wherein the single circuit device further includes the means for selectively deactivating and reactivating the first microprocessor circuit portion of the data processing means.

9. The microprocessor circuit according to claim 6, wherein the clocking speed of the first microprocessor circuit portion is at least twice that of the second microprocessor circuit portion.

10. The microprocessor circuit according to claim 6, wherein the means for communicatively coupling the first and second microprocessor circuit portions to each other comprises an interface means including a plurality of data latches, said data latches communicating with said first microprocessor circuit portion at said first clocking speed and with said second microprocessor circuit portion at said second clocking speed.

11. The microprocessor circuit according to claim 6, wherein the first microprocessor circuit portion is a 16-bit processor and the second microprocessor circuit portion is an 8-bit processor, the microprocessor circuit further comprising data storage means coupled to the 16-bit processor for at least temporarily storing data and program instructions, said data storage means including stored program instructions instructing said 16-bit processor to process data in response to the receipt of an activating control signal from the 8-bit processor.

12. The microprocessor circuit according to claim 6, wherein the first microprocessor circuit portion is a 16-bit processor and the second microprocessor circuit portion is an 8-bit processor, the second microprocessor

circuit portion further comprising storage means for controlling the operation of the 8-bit processor.

13. The microprocessor circuit according to claim 12, wherein the clocking speed of the 16-bit processor is at least twice that of the 8-bit processor.

14. The microprocessor circuit according to claim 13, wherein the 16-bit processor directly receives a string of data over a data bus from a scanning operation, while the 8-bit processor controls the access by the application processor to the data bus and further receives and transfers other periodic data to the 16-bit processor via the bidirectional communications means.

15. A microprocessor circuit for use in data processing apparatus comprising:

a first microprocessor subcircuit, including a first microprocessor block and timing means for driving the first microprocessor block at a first clocking speed;

a second microprocessor subcircuit, including a second microprocessor block and timing means for driving the second microprocessor block at a second clocking speed, the second clocking speed being functionally independent of said first clocking speed;

means for communicatively coupling the first and second microprocessor blocks to each other to bidirectionally pass data and control signals there between; and

means for selectively deactivating the first microprocesser block upon the first microprocessor block completing a data processing operation, and for selectively reactivating the first microprocessor block in response to a control signal from the second microprocessor block, whereby the first microprocessor block is coupled to operate intermittently to effect data processing operations and to become deactivated at the conclusion of the data processing operations.

16. The microprocessor circuit according to claim 15, wherein the second clocking speed is slower than the

first clocking speed.

17. The microprocessor circuit according to claim 15, wherein the first and second microprocessor blocks are discrete first and second microprocessor devices.

18. The microprocessor circuit according to claim 17, wherein the second clocking speed is slower than the first clocking speed.

19. The microprocessor circuit according to claim 18, wherein the means for communicatively coupling the first and second microprocessor devices to each other comprises an interface means including a plurality of data latches, said data latches communicating with said first microprocessor device at said first clocking speed and with said second microprocessor device at said second clocking speed.

20. The microprocessor circuit according to claim 18, wherein the first microprocessor device is a 16-bit processor and the second microprocessor device is an 8-bit processor, the microprocessor circuit further comprising data storage means for at least temporarily storing data and program instructions, the 16-bit processor being communicatively coupled to said data storage means for at least temporarily storing data and program instructions, said data storage means including stored program instructions instructing said 16-bit processor to process data in response to the receipt of an activating control signal from the 8-bit processor.

21. The microprocessor circuit according to claim 20, the microprocessor being disposed within a hand-held, portable data terminal unit including a keyboard, a display and a battery, wherein the 8-bit processor monitors the input signals from the keyboard and the display, transfers data signals received from the keyboard to the 16-bit processor for data processing operations, and receives processed data and instructional codes from the 16-bit processor in response to the transferred data signals.

22. The microprocessor circuit according to claim 21, wherein the 8-bit processor is directly coupled to a display contrast control circuit and includes means for controlling the contrast of the display of the data terminal unit.

23. The microprocessor circuit according to claim 21, wherein the 8-bit processor is coupled to a signal input terminal for receiving status input signals from a scanning module, and further comprises means for enabling the 16-bit processor to directly receive scanned data for processing in response to an input signal that the trigger of the scanning module has been activated.

24. The microprocessor circuit according to claim 21, wherein the means for communicatively coupling the 16-bit processor and the 8-bit processor to each other and the means for selectively deactivating and reactivating the 16-bit processor are formed on a single integrated circuit.

25. The microprocessor circuit according to claim 24, wherein the means for selectively deactivating and reactivating the 16-bit processor comprises means for selectively interrupting a clock signal to the 16-bit processor.

26. The hand-held data collection terminal unit according to claim 1, wherein the transceiver of the communications module is a spread spectrum transceiver, the data communications module including data modem circuit means coupled to the transceiver for communicating modulated data messages at a spread spectrum transceiver data rate bidirectionally to and from the spread spectrum transceiver, and for communicating demodulated, synchronous data messages at spread spectrum transceiver data rates to the communications interface, the communications interface comprising means for converting the synchronous data messages received from the spread spectrum transceiver to parallel data messages, and for converting parallel data messages to synchronous data

messages for communication to the modem circuit means, the microprocessor of the data communications module including means for converting the parallel data messages to serial data messages and for converting serial data messages to the parallel data messages.

27. The hand-held data collection terminal unit according to claim 26, wherein the communications module includes means for storing data messages, the data message storing means being communicatively coupled to the microprocessor of the communications module, the microprocessor of the communications module being operatively controlled to temporarily store received messages, to communicate received parallel data messages as asynchronous data messages to the microprocessor of the base module, and to communicate to the communications interface parallel data messages received as asynchronous data messages from the microprocessor of the base module.

28. The hand-held data collection terminal according to claim 26, wherein the microprocessor of the base module comprises first and second microprocessor subcircuits, the first subcircuit operable at a first clocking rate, the second microprocessor subcircuit operable at a second clocking rate which is less than the first clocking rate, the first microprocessor subcircuit being selectively operable for data processing operations and becoming deactivated upon concluding a data processing operation, the second microprocessor subcircuit monitoring and controlling operations of the base module and the communications module, and including means for selectively reactivating the operation of the first microprocessor subcircuit.

29. The hand-held data collection terminal according to claim 28, wherein the communications module includes means for storing data messages, the data message storing means being communicatively coupled to the microprocessor of the communications module, the microprocessor of the communications module being operatively controlled to

temporarily store received messages, to communicate received parallel data message as asynchronous data messages to the second microprocessor subcircuit of the base module, and to communicate to the communications interface parallel data messages received as asynchronous data messages from the second microprocessor subcircuit of the base module.

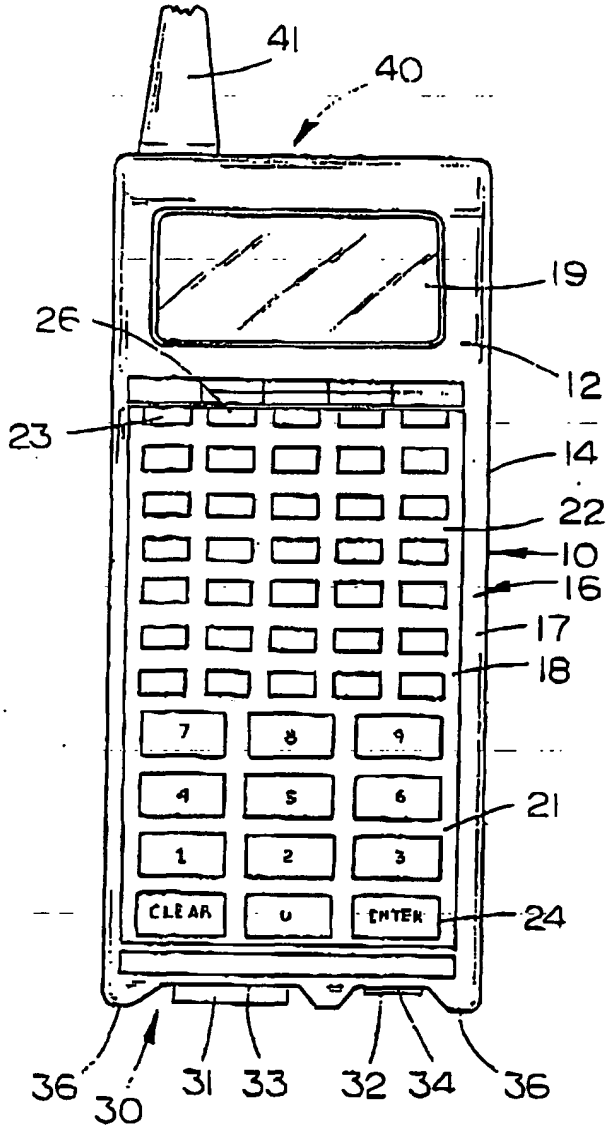
41
40
19
26
12
23
14
22
10
16
17
18
7
8
9
4
5
6
21
1
2
3
CLEAR
0
ENTER
24
36
30
31
33
32
34
36

FIG. 1

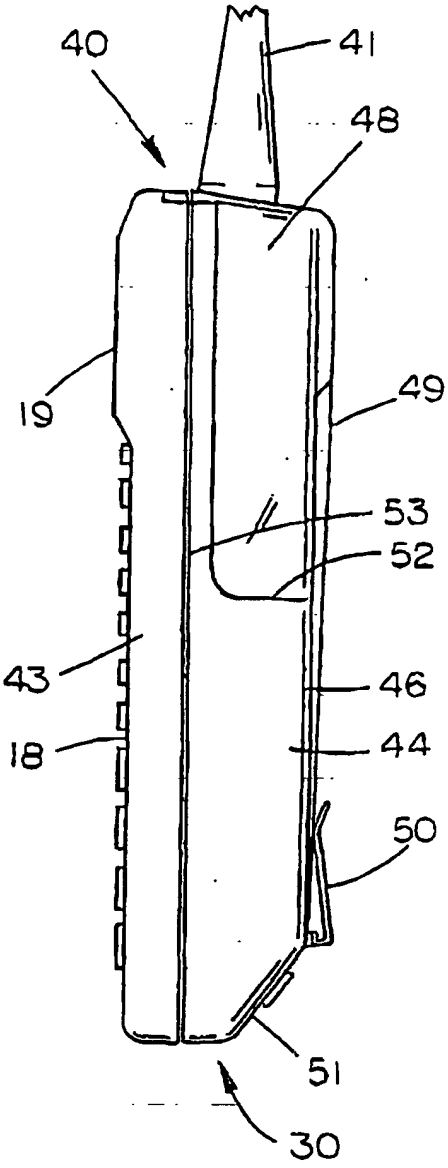
40
41
48
19
49
53
52
43
46
18
44
50
51
30

FIG. 2

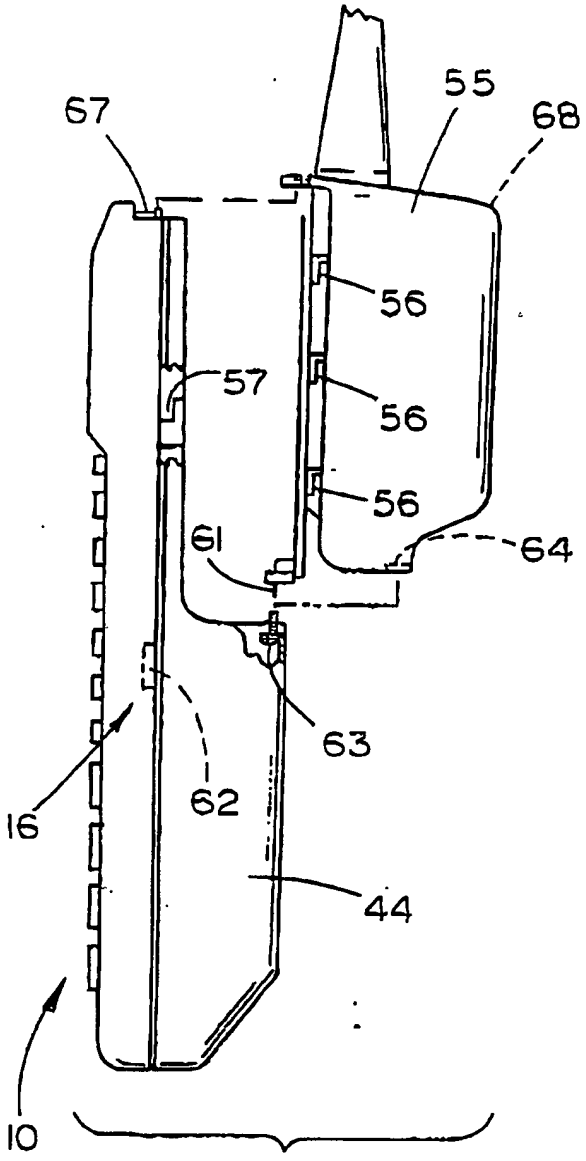

FIG. 3

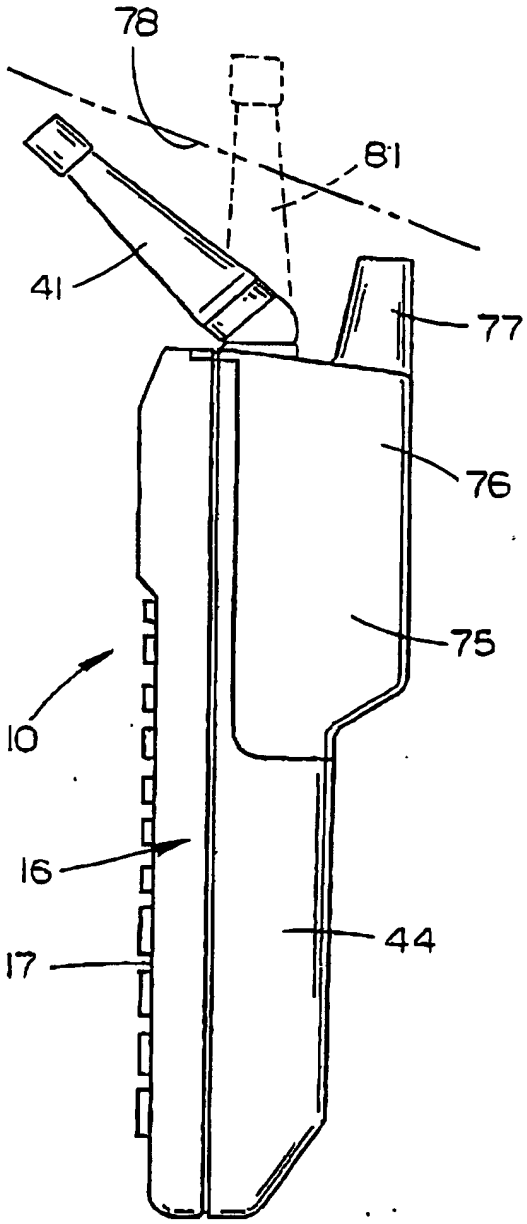

FIG. 4

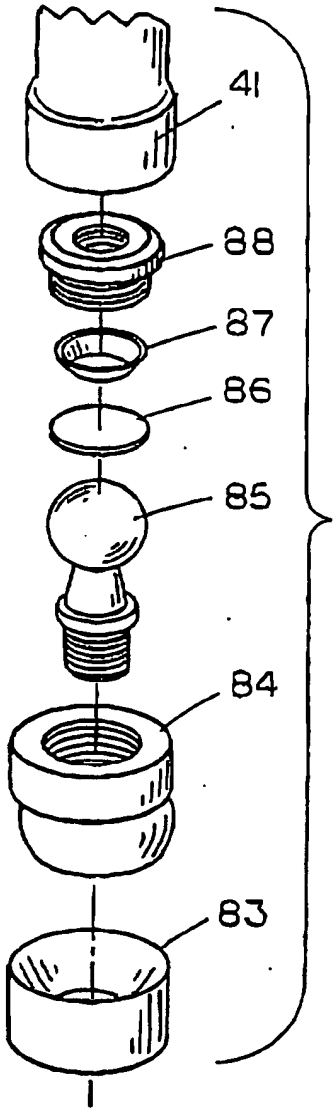

FIG. 5

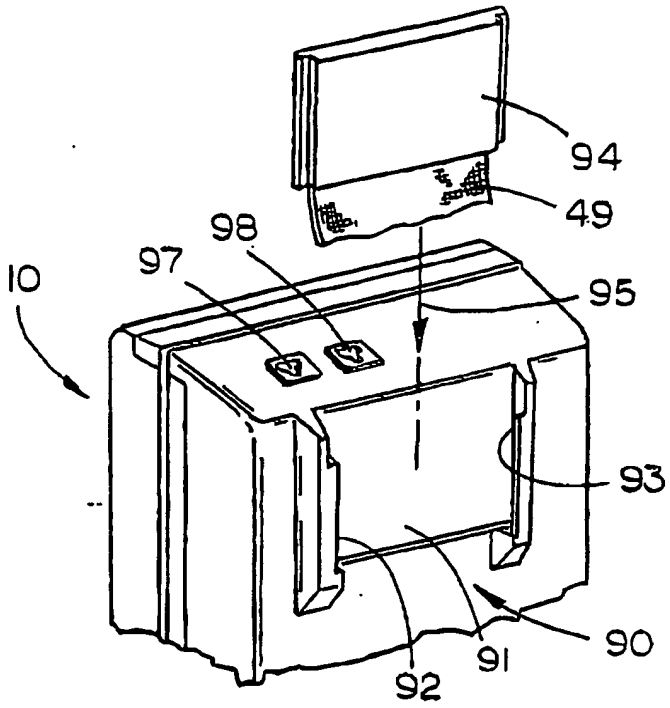

FIG. 7

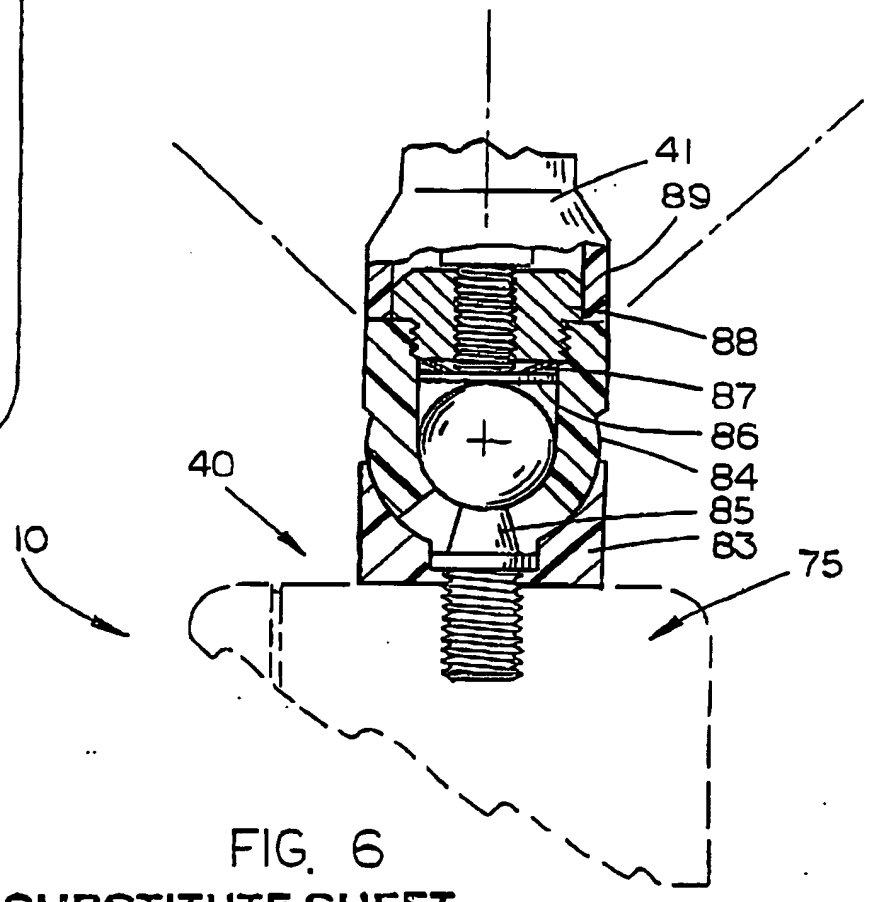

FIG. 6

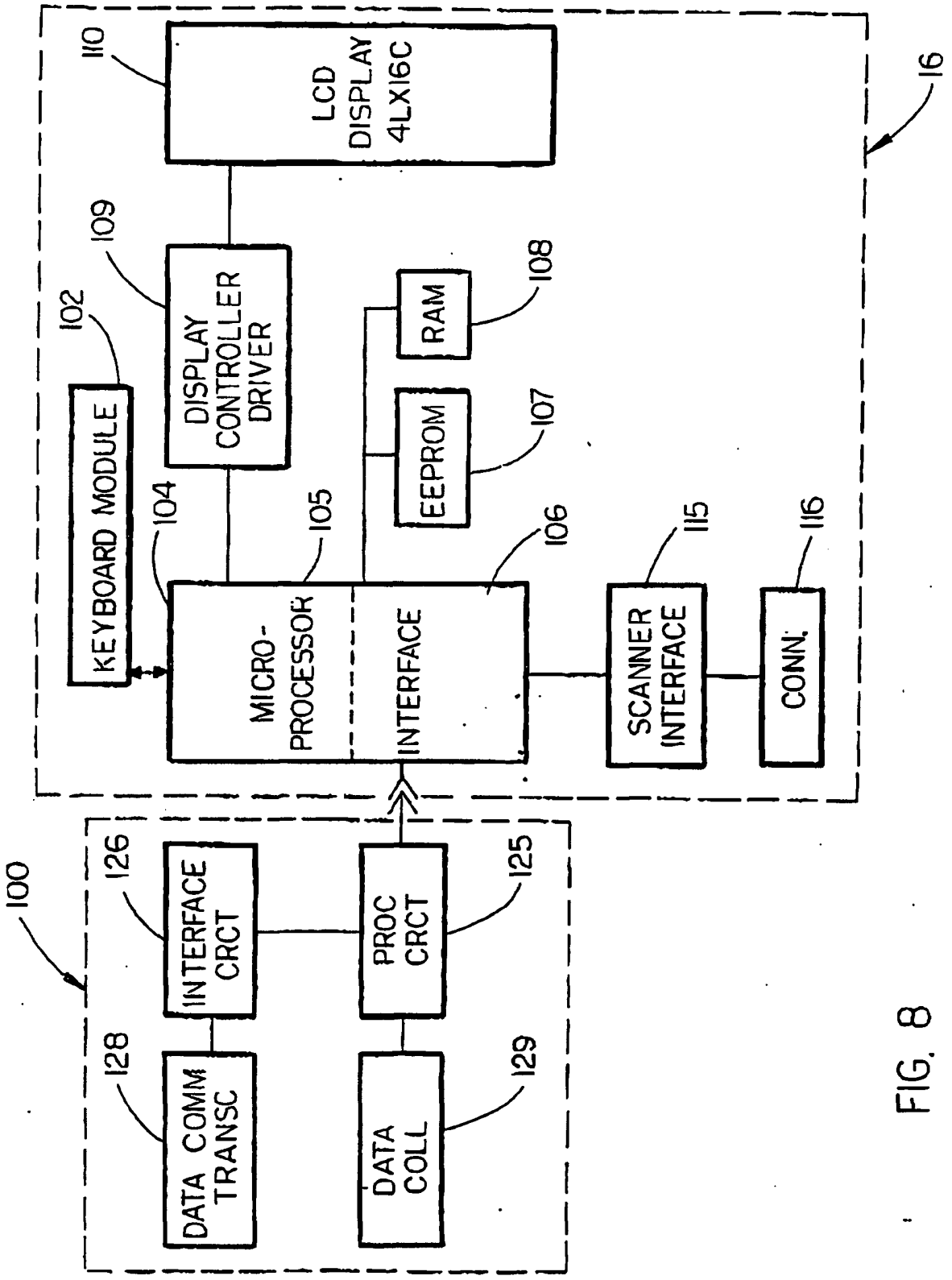
16
110
LCD DISPLAY 4LX16C
109
DISPLAY CONTROLLER DRIVER
102
KEYBOARD MODULE
104
105
106
MICRO-PROCESSOR
INTERFACE
RAM
108
EEPROM
107
115
SCANNER INTERFACE
116
CONN
100
126
INTERFACE CRCT
PROC CRCT
125
128
DATA COMM TRANSC
DATA COLL
129

FIG. 8

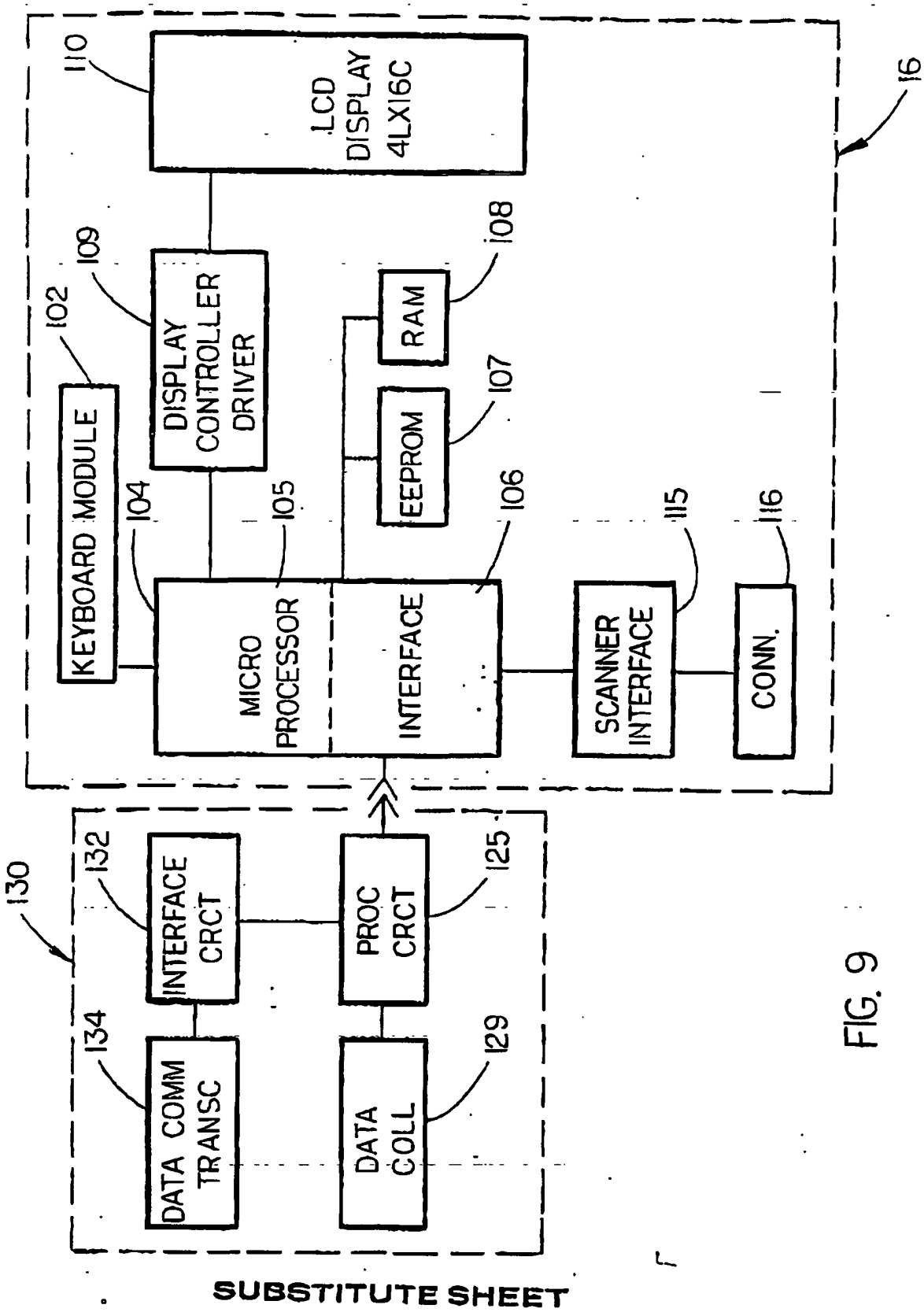
16
110
LCD DISPLAY 4LX16C
109
DISPLAY CONTROLLER DRIVER
108
RAM
102
KEYBOARD MODULE
107
EEPROM
104
105
106
115
116
MICRO PROCESSOR
INTERFACE
SCANNER INTERFACE
CONN.
130
132
INTERFACE CRCT
PROC CRCT
125
134
129
DATA COMM TRANSC
DATA COLL

FIG. 9

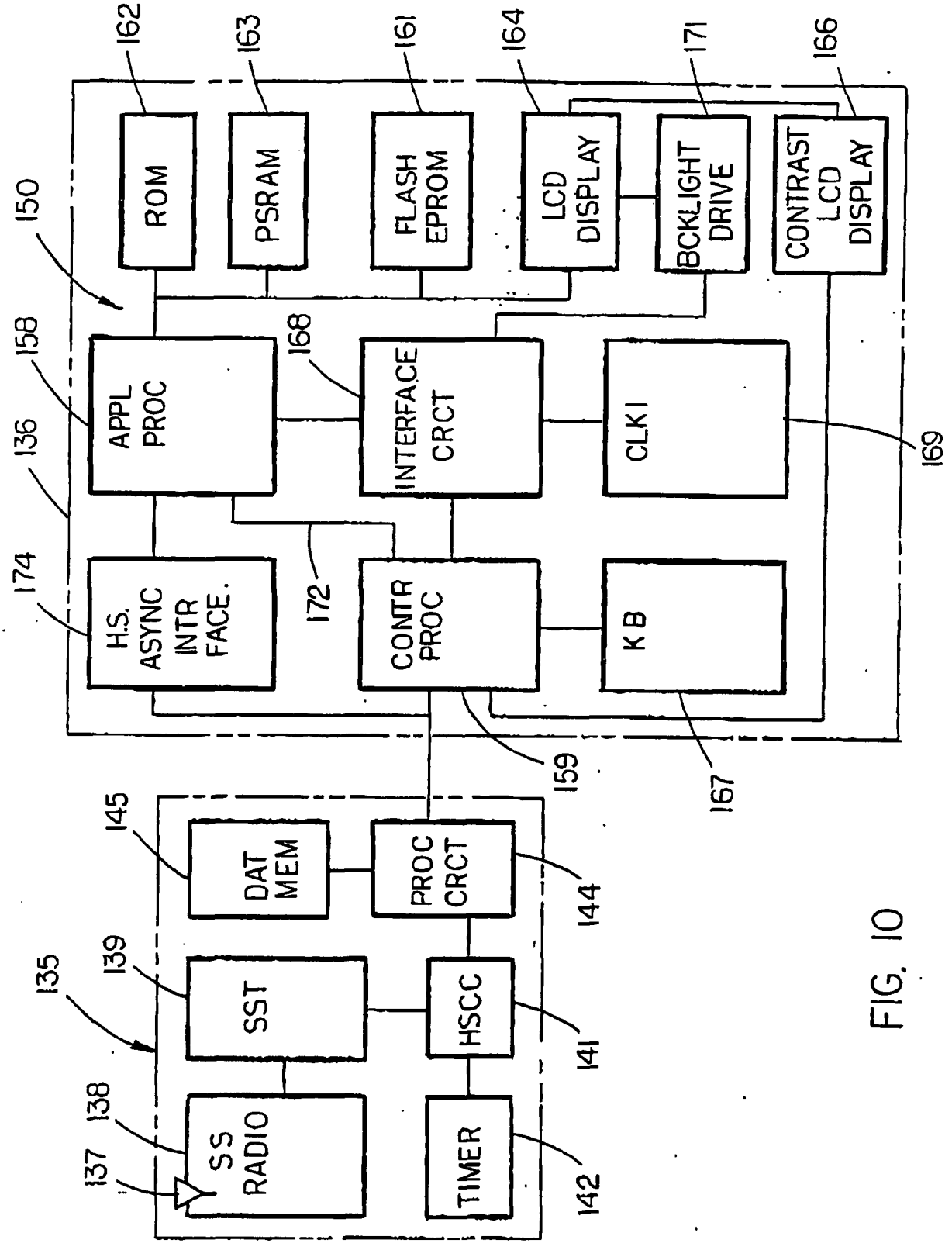
162
163
161
164
171
166
ROM
PSRAM
FLASH EPROM
LCD DISPLAY
BCKLIGHT DRIVE
CONTRAST LCD DISPLAY
150
158
168
APPL PROC
INTERFACE CRCT
CLK1
169
136
174
172
H.S. ASYNC INTR FACE.
CONTR PROC
K B
159
167
145
DAT MEM
PROC CRCT
144
139
135
SST
HSCC
141
138
137
SS RADIO
TIMER
142

FIG. 10

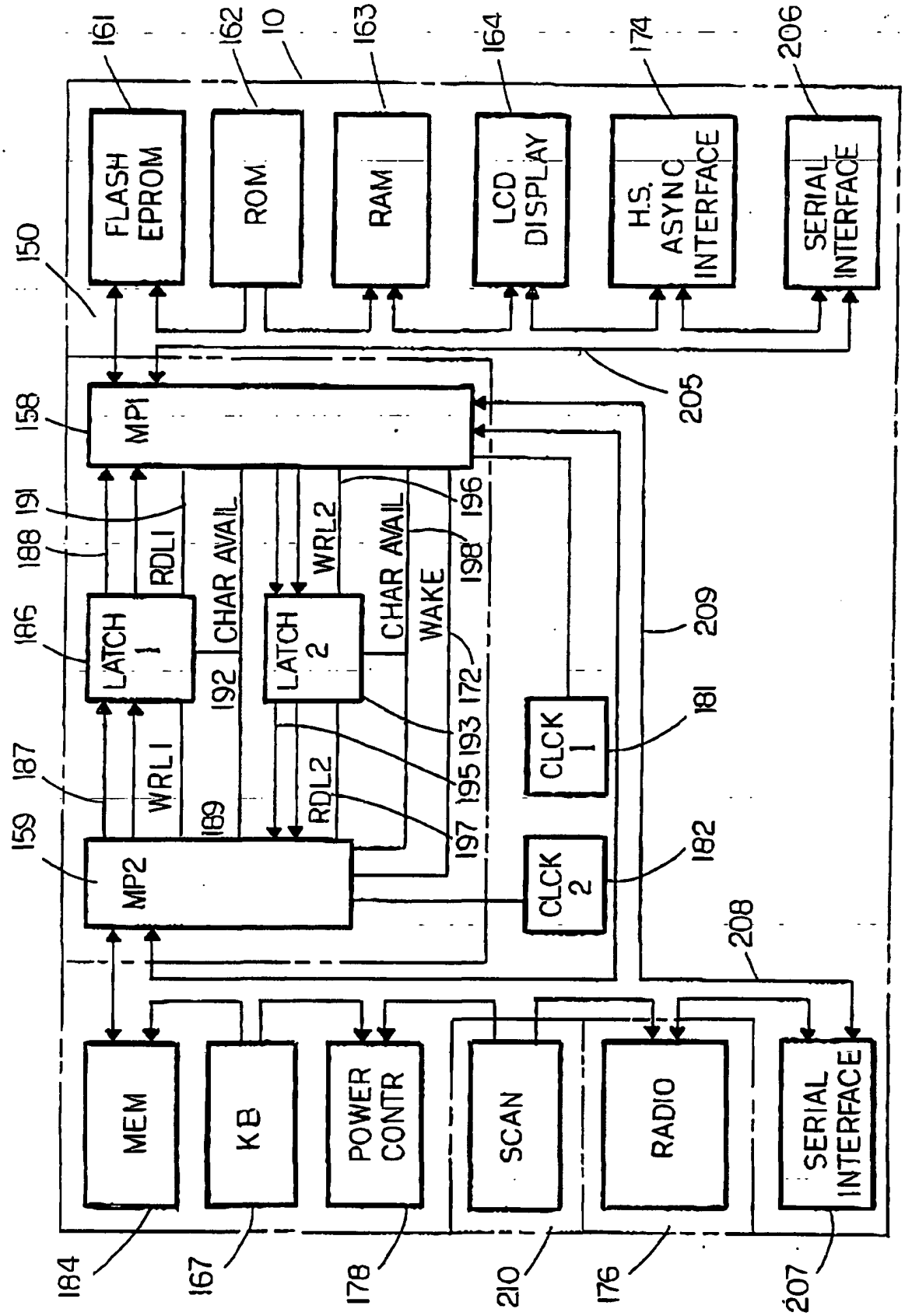
161
162
10
163
164
174
206
FLASH EPROM
ROM
RAM
LCD DISPLAY
H.S. ASYNC INTERFACE
SERIAL INTERFACE
150
205
158
MP1
191
188
RDL1
CHAR AVAIL
WRL2
CHAR AVAIL
196
198
186
LATCH 1
LATCH 2
WAKE
209
192
172
193
195
197
187
WRL1
RDL2
189
159
MP2
CLCK 1
CLCK 2
181
182
208
MEM
KB
POWER CONTR
SCAN
RADIO
SERIAL INTERFACE
184
167
178
210
176
207

FIG. 11

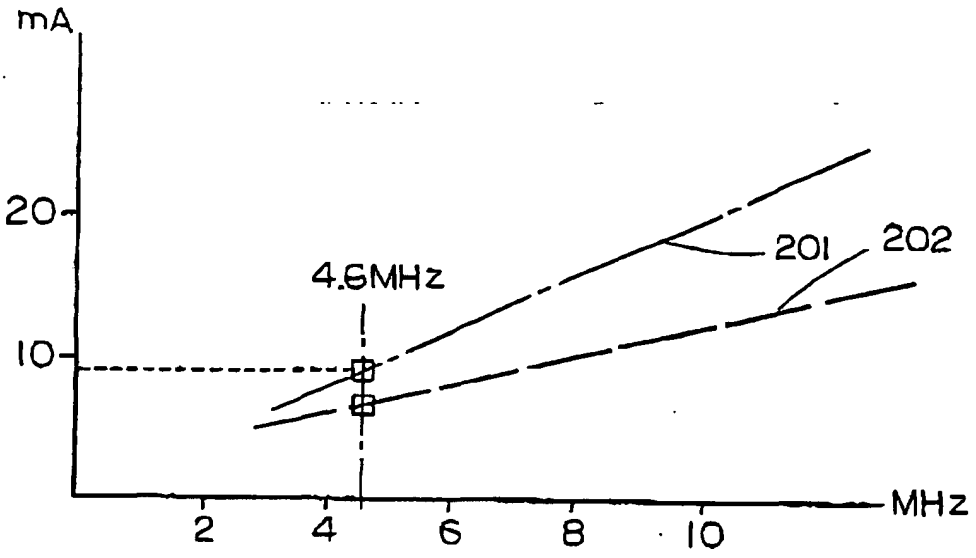
mA
20
10
4.6MHz
201
202
MHz
2
4
6
8
10

FIG. 12

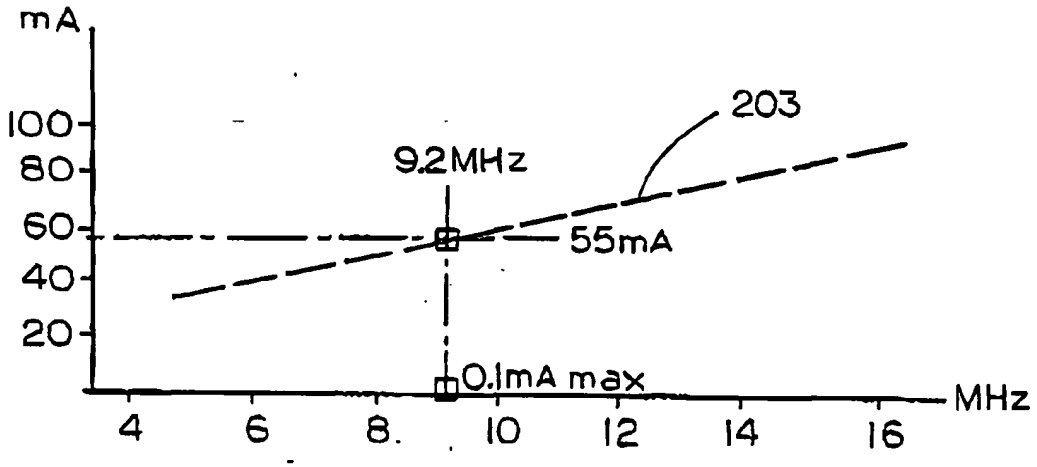
mA
100
80
60
40
20
9.2MHz
203
55mA
0.1mA max
MHz
4
6
8
10
12
14
16

FIG. 13

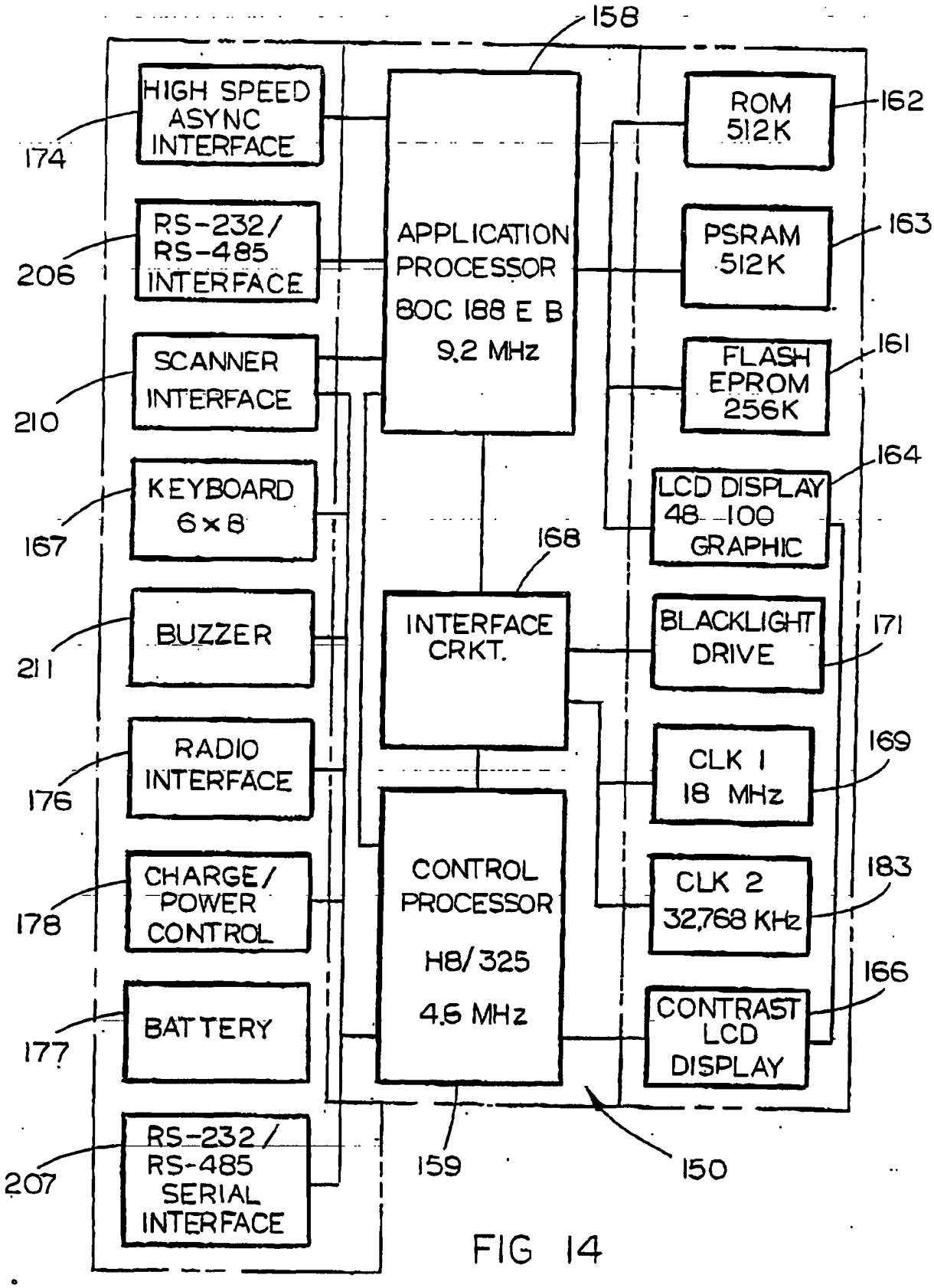
158
HIGH SPEED ASYNC INTERFACE
174
RS-232/ RS-485 INTERFACE
206
SCANNER INTERFACE
210
KEYBOARD 6x8
167
BUZZER
211
RADIO INTERFACE
176
CHARGE/ POWER CONTROL
178
BATTERY
177
RS-232/ RS-485 SERIAL INTERFACE
207
APPLICATION PROCESSOR 80C 188 E B 9.2 MHz
CONTROL PROCESSOR H8/325 4.6 MHz
159
INTERFACE CRKT.
168
150
ROM 512K
162
PSRAM 512K
163
FLASH EPROM 256K
161
LCD DISPLAY 48-100 GRAPHIC
164
BLACKLIGHT DRIVE
171
CLK 1 18 MHz
169
CLK 2 32,768 KHz
183
CONTRAST LCD DISPLAY
166

FIG 14

INTERNATIONAL SEARCH REPORT

International Application No. PCT/US92/01461

I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all) *

According to International Patent Classification (IPC) or to both National Classification and IPC

IPC (5): -G06K 7/10 G06F 15/24

U.S.Cl.: 235/385,454,472

II. FIELDS SEARCHED

Minimum Documentation Searched 7

Classification System	Classification Symbols
U.S.	235/385,454,472

Documentation Searched other than Minimum Documentation to the Extent that such Documents are included in the Fields Searched *

III. DOCUMENTS CONSIDERED TO BE RELEVANT *

Category *	Citation of Document, 11 with indication, where appropriate, of the relevant passages 12	Relevant to Claim No. 13
Y	US, A, 4,471,218 (CULP) 11 September 1984 See the entire document.	1-29
Y	US, A, 4,621,189 (KUMAR) 04 November 1986 See the entire document.	1-29
Y	US, A, 4,983,318 (KNOWLES) 08 February 1991 See the entire document.	1-29
Y,P	US, A, 5,047,614 (BIANCO) 10 September 1991 See the entire document.	1-29

* Special categories of cited documents: 10

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

IV. CERTIFICATION

Date of the Actual Completion of the International Search	Date of Mailing of this International Search Report
05 May 1992	16 JUN 1992
International Searching Authority	Signature of Authorized Officer
ISA/US	Harold Pitts

Form PCT/ISA/210 (Rev.11-87)

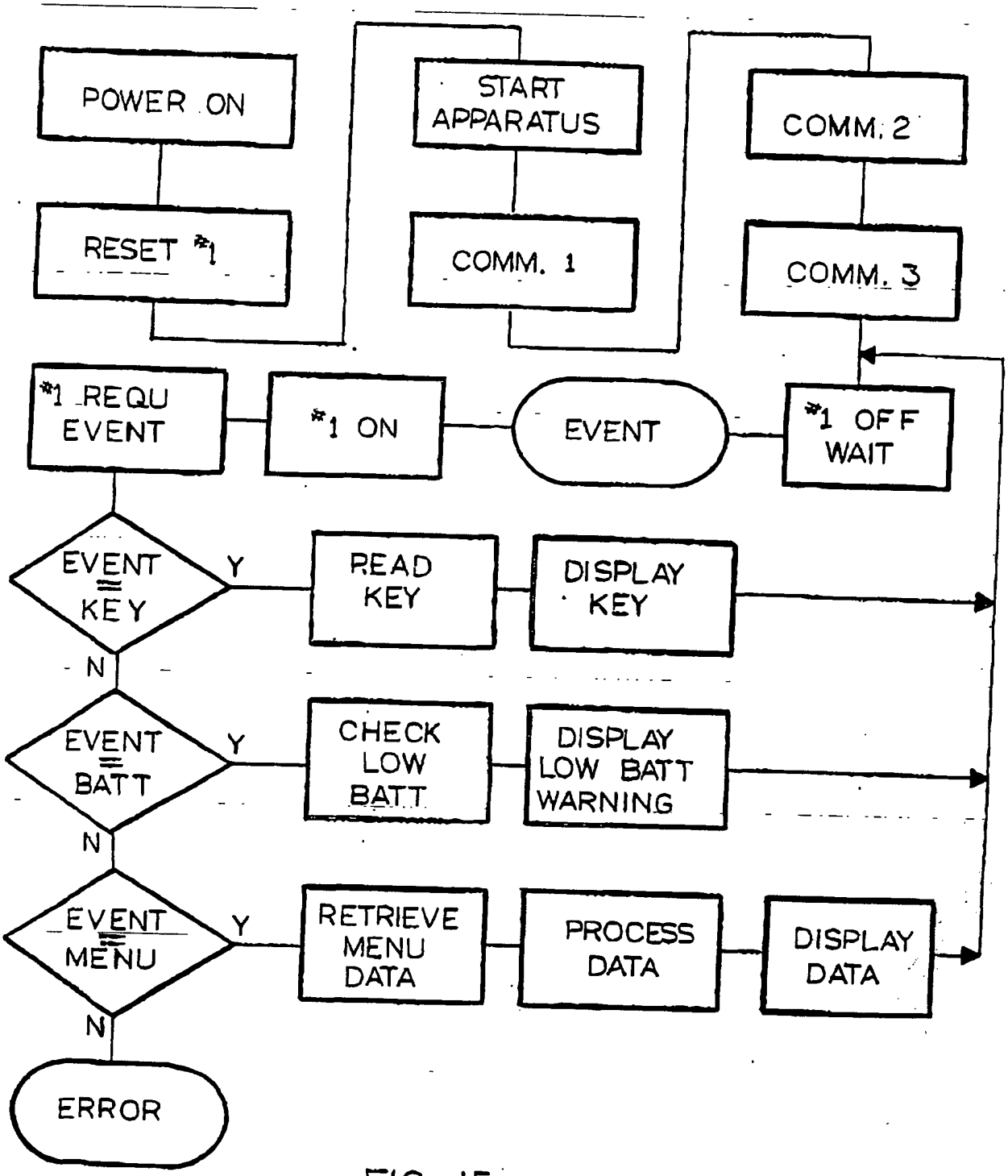
POWER ON
START APPARATUS
COMM. 2
RESET *1
COMM. 1
COMM. 3
*1 REQU EVENT
*1 ON
EVENT
*1 OFF WAIT
EVENT = KEY
Y
READ KEY
DISPLAY KEY
N
EVENT = BATT
Y
CHECK LOW BATT
DISPLAY LOW BATT WARNING
N
EVENT = MENU
Y
RETRIEVE MENU DATA
PROCESS DATA
DISPLAY DATA
N
ERROR

FIG. 15

EP 1720[illegible] (A)

(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) Publication number : **0 601 820 A1**

(12) EUROPEAN PATENT APPLICATION

(21) Application number : **93309777.6**

(51) Int. Cl.[5] : **H04Q 7/04**, H04B 7/26

(22) Date of filing : **06.12.93**

(30) Priority : **11.12.92 JP 331520/92**

(43) Date of publication of application :
15.06.94 Bulletin 94/24

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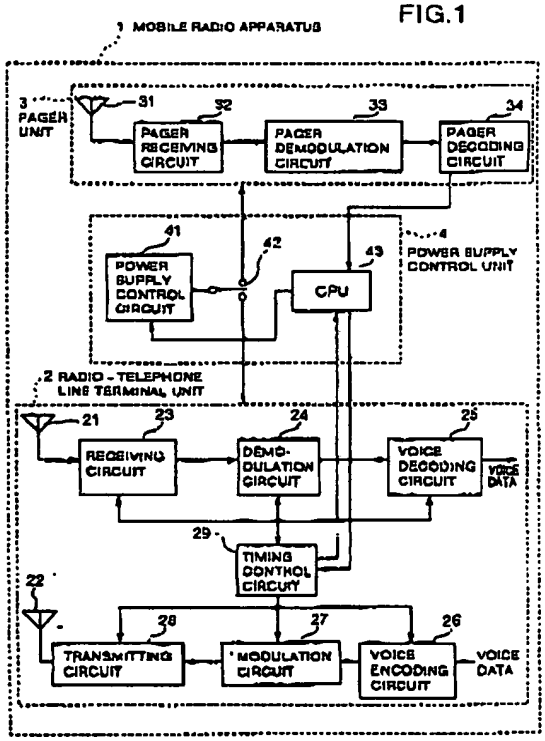
(54) Mobile radio apparatus.

(57) When a power supply of a mobile radio apparatus (1) is turned on, a power supply change-over switch (42) of a power supply control unit (4) is changed over to the side of a pager unit (3) to turn on only a power supply of the pager unit (3), so that a pager network which does not require position registration is utilized to perform intermittent receiving operation with low power consumption. When there is an incoming call to the pager unit (3), a CPU (43) of the power supply control unit (4) receives an incoming control signal from a pager decoding circuit (34) and changes over the power supply change-over switch (42) to the side of a radio-telephone line terminal unit (2) to turn on the radio telephone line terminal unit (2) and turn off the pager unit (3). The CPU (43) sends a control signal to a timing control circuit (29) of the radio-telephone line terminal unit (2) so that the position registration is performed by utilizing a mobile radio network and an operation mode of the mobile radio apparatus proceeds to a usual talking mode. After a pager calling has been performed in a calling side, the mobile radio apparatus is called by the portable telephone number and talking is then is made. When the talking has been finished, the CPU (43) receives a control signal from the timing control circuit (29) and changes over the power supply change-over switch (42) to the side of the pager unit (3) again to turn on the pager unit (3) to enter a waiting state for reception.

FIG.1



EP 0 601 820 A1

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to a mobile radio apparatus for a portable telephone and the like which is desired to be operated with low power consumption.

Description of the Related Art

Fig. 7 is a schematic diagram illustrating a conventional mobile radio apparatus. As an example of the mobile radio apparatus, a portable telephone is shown. In Fig. 7, reference numerals 21 and 22 denote antennas. The antenna 21 is a receiving antenna, while the antenna 22 is operated as a transmitting antenna upon transmission and is operated as a receiving antenna upon reception to perform the diversity reception together with the antenna 21. Numeral 23 denotes a receiving circuit for amplifying a received signal. Numeral 24 denotes a demodulation circuit which demodulates a baseband signal from the received signal to obtain a digital data and reproduces a clock from the received signal. Numeral 25 denotes a voice decoding circuit which converts the digital data into an analog voice signal. Numeral 26 denotes a voice encoding circuit for converting the analog voice signal into a digital data. Numeral 27 denotes a modulation circuit for performing modulation in accordance with modulation systems by using the digital data. Numeral 28 denotes a transmitting circuit for amplifying a modulated signal. Numeral 30 denotes a timing control circuit for controlling the timing for the whole mobile radio apparatus.

Among operations of the mobile radio apparatus shown in Fig. 7, operation of an intermittent receiving mode upon waiting for reception and a position registration, specifically, is now described. Upon waiting for reception, objects to be supplied with the clock from the timing control circuit 30 are minimized and a power supply for supplying power to the receiving circuit 23 and the demodulation circuit 24 is turned on only during slots for necessary information, while the voice decoding circuit 25, the voice encoding circuit 26, the modulation circuit 27 and the transmitting circuit 28 are changed into a standby mode. In this manner, the mobile radio apparatus is switched to the intermittent receiving mode. In the intermittent receiving mode, several intermittent receiving operations are made for several hundred milliseconds and only necessary information is received to reduce the power consumption during waiting for reception and lengthen a time capable of waiting for reception for one charging of a battery. When a simultaneous calling area in which a user of the mobile radio apparatus is located is changed in accordance with variation of a reception level due to movement of the user, the position registration is required for recognizing a position of the mobile radio apparatus to a base station of a portable telephone network for the changed simultaneous calling area and transmission is made for the position registration. The transmission is made only upon the position registration operation, while it is necessary to reduce the power consumption at this time as small as possible.

However, in the conventional mobile radio apparatus constituted by the portable telephone by way of example, the intermittent receiving operation is performed to lengthen the time capable of waiting for reception for one charging of the battery, while the waitable time is only about several ten hours and the charging of the battery is required frequently.

Further, in order to reduce the power consumption, the mobile radio apparatus including a pager combined with the portable telephone is disclosed in JP-A-61-67336 and JP-A-5-102924. In such a mobile radio apparatus, only the pager unit is operated during the waiting for reception and the portable telephone is supplied with power after a calling signal has been received, so that reduction of the power consumption during the waiting for reception is effected.

In the abovementioned papers, however, the position registration in case where the user of the mobile radio apparatus is moved is not described. Generally, in the mobile radio apparatus such as the portable telephone, each time the simultaneous calling area in which the user of the portable telephone is located is changed to a new area, the position registration is required to recognize the position of the user of the portable telephone to the base station of the portable telephone network for the new area. Although one transmission time for the position registration is short, the power consumption for each transmission is large and this is a great problem encountered when the power consumption of the whole apparatus is made smaller.

SUMMARY OF THE INVENTION

The present invention is to solve the above problem in the prior art and an object of the present invention is to provide a mobile radio apparatus in which a power supply of a portable telephone unit is off and only a pager unit is operated during waiting for reception while a power supply of the pager unit is off and only the portable telephone unit is operated at need, and the frequency of the position registration is reduced to minimize the power consumption.

In order to achieve the object, according to the present invention, the mobile radio apparatus comprises a radio-telephone line terminal unit, a pager unit and a power supply control unit. During waiting for reception of a radio-telephone, a power supply of the radio-telephone line terminal unit is off and only a power supply of the pager unit which does not re-

quire the position registration is on. When there is an incoming call for the pager unit, the power supply control unit turns on the power supply of the radio-telephone line terminal unit and turns off the power supply of the pager unit and then causes the radio-telephone line terminal unit to perform the position registration and a mode is changed to a talking mode to make talking. When the talking is finished, the power supply of the radio-telephone line terminal unit is turned off and the power supply of the pager unit is turned on again by means of control of the power supply control unit to enter the waiting state for reception again.

According to the present invention, since the power supply of the radio-telephone line terminal unit is off in the waiting state and the frequency of transmission for the position registration necessary for the radio-telephone line terminal unit is reduced remarkably, the power consumption of the mobile radio apparatus is reduced greatly.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a block diagram schematically illustrating a mobile radio apparatus according to a first embodiment of the present invention;

Fig. 2 is a flow chart showing operation of the mobile radio apparatus according to the first embodiment;

Fig. 3 is a block diagram schematically illustrating a mobile radio apparatus according to a second embodiment of the present invention;

Fig. 4 is a flow chart showing operation of the mobile radio apparatus according to the second embodiment;

Fig. 5 is a diagram illustrating a calling procedure of the mobile radio apparatus according to the embodiments of the present invention;

Fig. 6 is a schematic diagram illustrating a configuration of a communication network including the mobile radio apparatus according to the embodiments of the present invention; and

Fig. 7 is a block diagram schematically illustrating a conventional mobile radio apparatus.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Fig. 1 schematically illustrating a mobile radio apparatus according to a first embodiment of the present invention. In Fig. 1, numeral 1 denotes a mobile radio apparatus, 2 a radio-telephone line terminal unit (hereinafter referred to as a line terminal unit 2 in description of the embodiment), 3 a pager unit, and 4 a power supply control unit for controlling turning-on-and-off of power supplies for the line terminal unit 2 and the pager unit 3. The mobile radio apparatus 1 comprises the line terminal unit 2, the pager unit 3 and the power supply control unit 4. In the embodiment, the line terminal unit 2 is described as a portable telephone as an example, however, the line terminal unit 2 may be a terminal unit of other kinds capable of being connected to a radio-telephone line, such as, for example, a picture communication terminal unit and a data communication terminal unit. The line terminal unit 2 includes blocks designated by reference numerals 21 to 29. The blocks designated by reference numerals 21 to 28 are the same blocks as those constituting the conventional mobile radio apparatus shown in Fig. 7 and accordingly description thereof is omitted by designating them by the same reference numerals. Reference numeral 29 denotes a timing control circuit for controlling the timing for the blocks of the line terminal unit 2. The timing control unit 29 is different from the timing control unit 30 of Fig. 7 in that the timing control unit 29 is operated by control of the power supply control unit 4. The pager unit 3 includes elements designated by reference numerals 31 to 34. Reference numeral 31 denotes an antenna of the pager unit for receiving electric wave for the pager unit and which is provided separately from the antennas 21 and 22 of the line terminal unit 2. Numeral 32 denotes a pager receiving circuit for amplifying a pager signal received by the pager antenna 31. Numeral 33 denotes a pager demodulation circuit for demodulating the pager signal. Numeral 34 denotes a pager decoding circuit for decoding the demodulated pager signal to produce an incoming control signal. The power supply unit 4 includes elements designated by reference numerals 41 to 43. Numeral 41 denotes a power supply control circuit for controlling to supply a supply voltage from a battery (not shown) to any of the line terminal unit 2 and the pager unit 3 in accordance with a control signal. Numeral 42 denotes a power supply change-over switch which is controlled by the power supply control circuit 41 to be changed over so that the battery power supply is connected to either the line terminal unit 2 or the pager unit 3. Numeral 43 denotes a CPU for controlling operation of each of portions of the mobile radio apparatus 1 in response to signals from the timing control circuit 29, the pager decoding circuit 34 and a power supply switch (not shown) of the mobile radio apparatus 1.

Fig. 2 is a flow chart showing operation of the first embodiment. Referring now to Figs. 1 and 2, operation of the first embodiment is described. When the power supply of the mobile radio apparatus 1 is turned on by means of a power supply switch not shown (step S1), the power supply change-over switch 42 is changed over to the side of the pager unit 3 by means of the CPU 43 and the power supply control circuit 41 of the power supply control unit 4 to turn on only the power supply of the pager unit 3 (step S2) so that the intermittent receiving operation of the pager signal is made with the low power consumption

by using the pager network which does not require the position registration. When there is an incoming call to the pager unit 3 during waiting for reception (step S3), the CPU 43 receives an incoming control signal from the pager decoding circuit 34 to control the power supply control unit 41 so that the power supply change-over switch 42 is changed over to the side of the line terminal unit 2 (step S4). Consequently, the line terminal unit 2 is powered on and the pager unit 3 is powered off (step S5). Thus, the CPU 43 sends the control signal to the timing control circuit 29 of the line terminal unit 2 to thereby perform the position registration to cause the base station of the portable telephone network of the area to recognize the position of the portable telephone (step S6) and the line terminal unit 2 is moved to the usual talking mode (step S7). After the pager calling has been made, the calling side or party dials the telephone number of the portable telephone to call it, so that an incoming call arrives at the portable telephone (step S8) to thereby be able to make talking between the calling side and the called portable telephone (step S9). When the talking has been finished (step S10), the CPU 43 receives the control signal from the timing control circuit 29 (path P1) and changes over the power supply change-over switch 42 to the pager unit 3 again so that the pager unit 3 is powered on and the line terminal unit 2 is powered off to enter the waiting state for reception of the pager signal (step S2).

Fig. 3 schematically illustrates a mobile radio apparatus according to a second embodiment of the present invention. In Fig. 3, a timer 44 is added to the power supply control unit 4 and performs timing control by means of the CPU 43. In Fig. 3, elements except for the timer 44 are those having the same functions as in the first embodiment and description thereof is omitted by designating them by the same reference numerals.

Fig. 4 is a flow chart showing operation of the second embodiment. Referring now to Figs. 3 and 4, operation of the second embodiment is described. In Fig. 4, the steps S1 to S10 have the same operation as those of the first embodiment shown in Fig. 2 and description thereof is omitted by designating them by the same step numbers. In Fig. 4, when the line terminal unit 2 is moved to the usual talking mode (step 7), the timer 44 of the power supply control unit 4 starts its operation in accordance with the control of the CPU 43 (step S11). The CPU 43 monitors the timer 44 (step S12) and when an incoming call arrives at the line terminal unit 2 within a predetermined time period from the start of the operation of the timer 44 (step S8), talking is made (step S9). When there is no incoming call within the predetermined time period (path P2) or when an incoming call arrives at the line terminal unit 2 once to thereby make talking (step S9) and the talking has been finished (step S10 and path P3), the CPU 43 receives the control signal from the timer 44 and the timing control circuit 29 (path P1) and the power supply change-over switch 42 is changed over to the side of the pager unit 3 again, so that the pager unit 3 is turned on and the line terminal unit 2 is turned off to thereby enter the waiting state for reception of the pager signal (step S2).

Fig. 5 illustrates a calling procedure of the mobile radio apparatus 1 according to the first and second embodiments. Fig. 6 schematically illustrates a configuration of a communication network for the radiotelephone and the pager including the mobile radio apparatus 1 according to the first and second embodiments. Letters (A) to (L) shown in Fig. 5 correspond to letters (A) to (L) shown in Fig. 6, respectively.

In Fig. 6, reference numeral 61 denotes a fixed telephone, 62 a portable telephone, 63 a base station for the portable telephone, 64 a public telephone network, 65 a base station for a mobile radio apparatus, 66 the mobile radio apparatus, and 67 a base station for a pager.

Referring now to Figs. 5 and 6, the calling procedure of the mobile radio apparatus according to the first and second embodiments is described. The calling side or party calls the mobile radio apparatus 1 through the pager network (process A). Thus, the pager base station performs the simultaneous calling for the pager (process B). The mobile radio apparatus 1 receives an incoming pager signal (process C), and turns on the power supply of the line terminal unit 2 and turn off the power supply of the pager unit 3 (process D) so that the position registration is performed (process E). Then, the mobile radio apparatus 1 is moved to the usual talking mode (process F). Thus, the calling side cuts off the telephone once and performs the calling of the portable telephone (process G). Thus, the simultaneous calling is performed through the public telephone network as the portable telephone (process H), so that an incoming portable telephone call is received by the mobile radio apparatus 1 (process J). Talking is then made (process K) and when the talking has been finished (process L) and the mobile radio apparatus is moved to the waiting state for reception, the mobile radio apparatus turns off the power supply of the line terminal unit 2 and turns on the power supply of the pager unit 3 again.

As described above, according to the first and second embodiments, the power supply of the line terminal unit 2 is turned off and only the power supply of the pager unit 3 is turned on during waiting for reception to thereby enter the waiting state for reception for the pager which does not require the position registration. When an incoming signal of the pager is received, the line terminal unit 2 is turned on and the pager unit 3 is turned off to perform the position registration and move to the usual talking mode. Thus, since the power consumption by the transmission for

the position registration during waiting for reception can be removed entirely, the power consumption of the mobile radio apparatus 1 can be reduced and the waiting time for reception by one charging can be lengthened.

In the first and second embodiments, the calling side first performs the pager calling and then performs the calling of the portable telephone, while one-to-one correspondence of the pager number and the telephone number of the portable telephone can cause the mobile radio apparatus 1 to be automatically moved to the talking mode only by performing the pager calling.

According to the present invention, as apparent from the embodiments, the mobile radio apparatus comprises the pager unit and the power supply control unit in addition to the radio-telephone line terminal unit and turns off the power supply of the line terminal unit during waiting for reception of the radio-telephone line to wait for reception of an incoming pager signal. When there is the incoming signal to the pager unit, the power supply control unit turns on the power supply of the line terminal unit and performs the necessary position registration. Accordingly, since it is not necessary to perform the intermittent receiving operation or the transmission for the position registration that is always performed during waiting for reception of the conventional mobile radio apparatus, the power consumption during waiting for reception can be reduced greatly and the time capable of waiting for reception by one charging can be also lengthen greatly so that the usable time of the mobile radio apparatus can be made long.

Claims

1. A mobile radio apparatus comprising:

a radio-telephone line terminal unit (2) for talking with one of a plurality of radio-telephone base stations in accordance with a position of said mobile radio apparatus, said radio-telephone line terminal unit (2) including a timing control circuit (29) for controlling operation of said radio-telephone line terminal unit and for producing a first control signal when talking of said radio-telephone line terminal unit is finished;

a pager unit (3) for receiving a calling signal from at least one pager base station, said pager unit (3) including a decoding circuit (34) for producing a second control signal when said pager unit (3) receives a calling signal specifying said pager unit;

a power supply control circuit (41) and selecter means (42), when said mobile radio apparatus is energized, for supplying electric power to one of said radio-telephone line terminal unit (2) and said pager unit (3);

a control circuit (43) for controlling said power supply control circuit (41) to (a) supply electric power to said pager unit (3) when said mobile radio apparatus comes to be energized, to (b) supply electric power to said radio-telephone line terminal unit (2) when said control circuit (43) receives said second control signal and to (c) supply electric power to said pager unit (3) again when said control circuit (43) receives said first control signal, and for controlling said timing control circuit (29) to cause said radio-telephone line terminal unit (2) to perform position registration for acknowledging the position of said mobile radio apparatus to at least one of said portable telephone base stations when said control circuit (43) receives said second control signal.

2. A mobile radio apparatus according to claim 1, further comprising timer means (44), wherein said control circuit (43) causes said timer means (44) to start its measurement of time when said control means (43) receives said second control signal, and controls said power supply control circuit (41) to supply electric power to said pager unit (3) again when an elapsed time represented by an output signal of said timer means exceeds a predetermined time period while there is no incoming signal to said radio-telephone line terminal unit (2) from said radio-telephone base station.

3. A mobile radio apparatus according to claim 1, wherein a calling number of said pager unit is identical with a telephone number of said radio-telephone line terminal unit so that when said pager unit (3) receives a signal calling said pager unit, said radio-telephone line terminal unit (2) also receives a signal calling said radio-telephone line terminal unit.

4. A mobile radio apparatus according to claim 2, wherein a calling number of said pager unit is identical with a telephone number of said radio-telephone line terminal unit so that when said pager unit (3) receives a signal calling said pager unit, said radio-telephone line terminal unit (2) also receives a signal calling said radio- telephone line terminal unit.

FIG.1

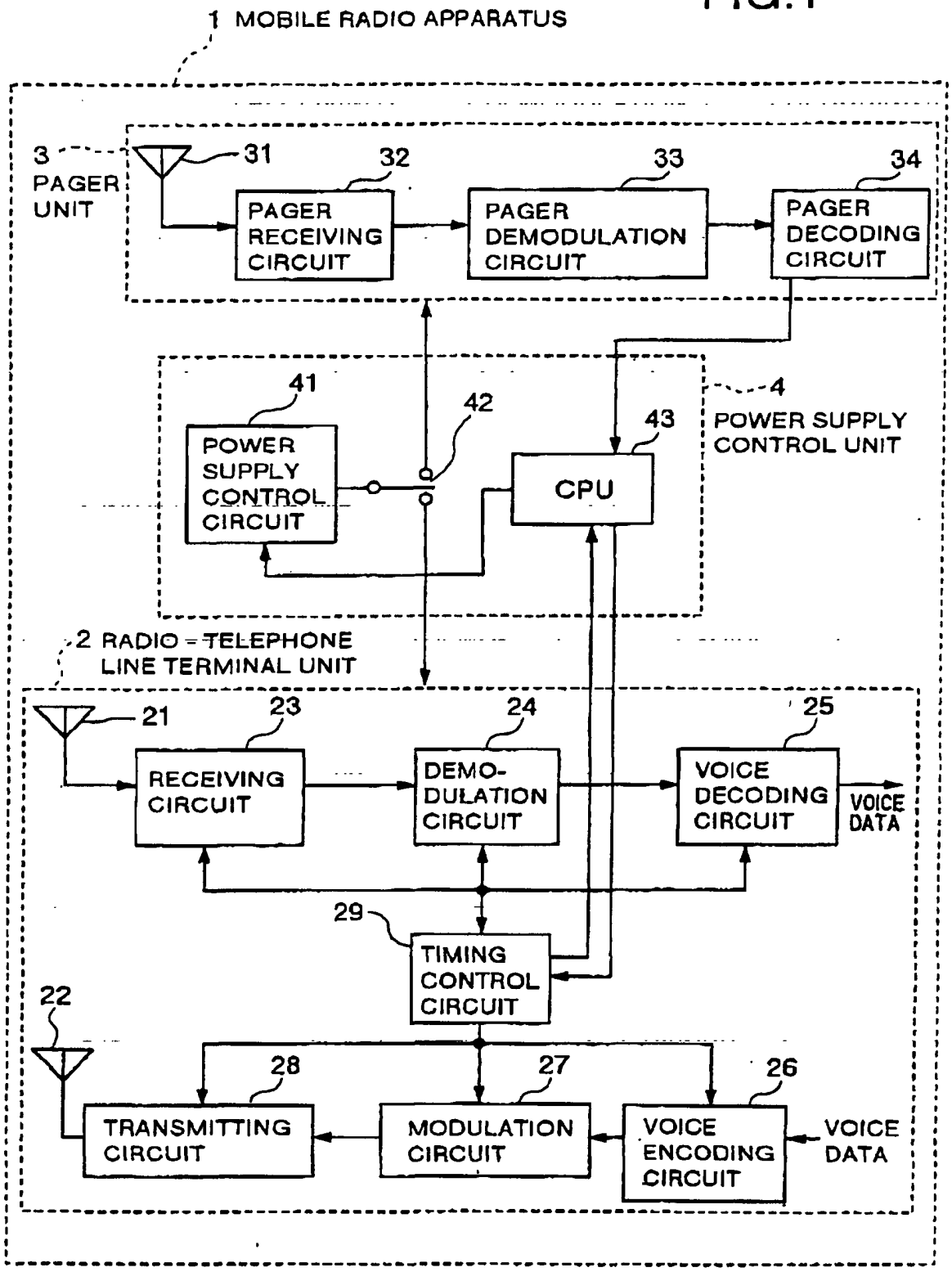

1 MOBILE RADIO APPARATUS
3 PAGER UNIT
31
32
PAGER RECEIVING CIRCUIT
33
PAGER DEMODULATION CIRCUIT
34
PAGER DECODING CIRCUIT
41
POWER SUPPLY CONTROL CIRCUIT
42
43
CPU
4 POWER SUPPLY CONTROL UNIT
2 RADIO = TELEPHONE LINE TERMINAL UNIT
21
23
RECEIVING CIRCUIT
24
DEMO-DULATION CIRCUIT
25
VOICE DECODING CIRCUIT
VOICE DATA
29
TIMING CONTROL CIRCUIT
22
28
TRANSMITTING CIRCUIT
27
MODULATION CIRCUIT
26
VOICE ENCODING CIRCUIT
VOICE DATA

FIG.2

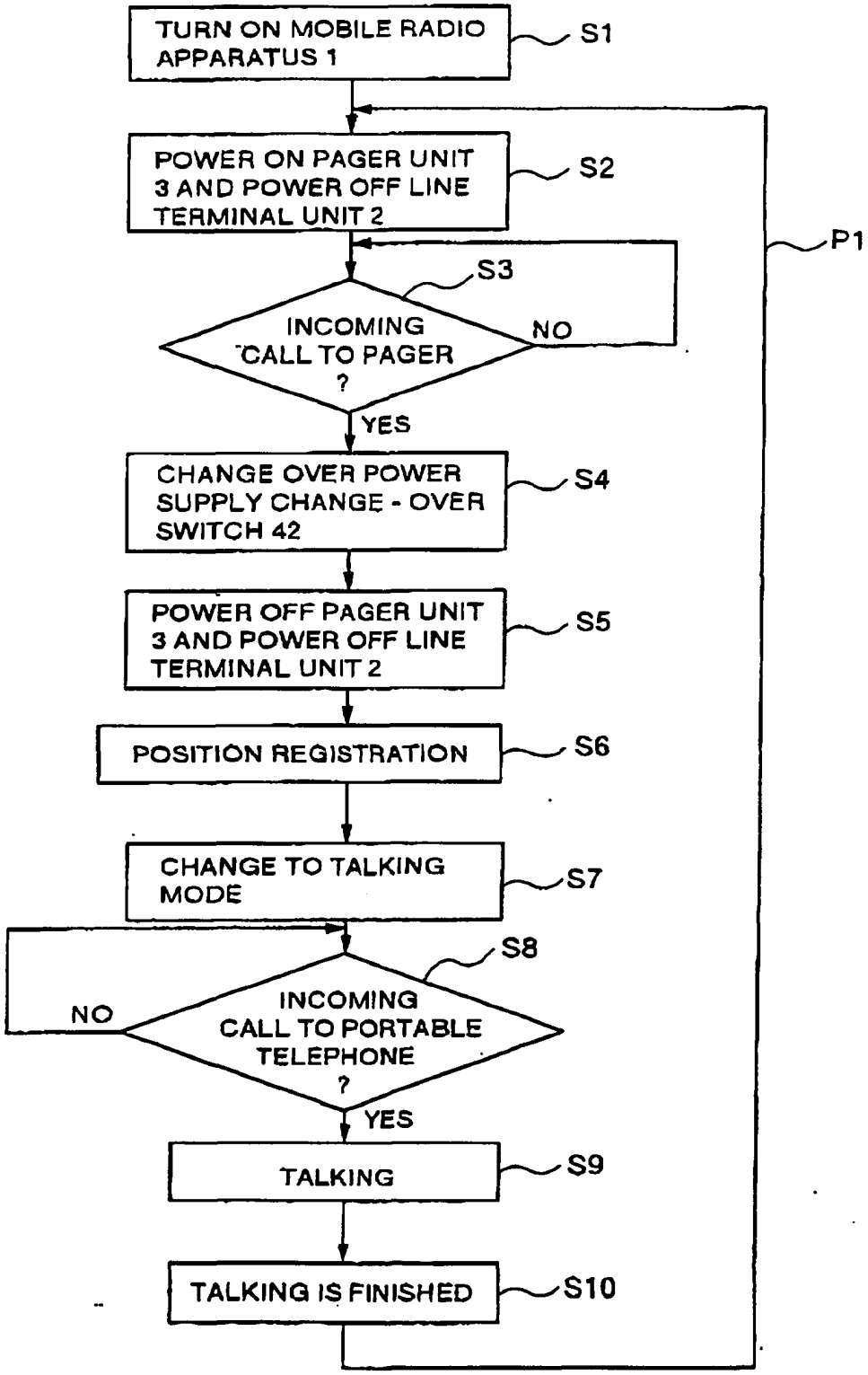

TURN ON MOBILE RADIO APPARATUS 1
S1
POWER ON PAGER UNIT 3 AND POWER OFF LINE TERMINAL UNIT 2
S2
P1
S3
INCOMING CALL TO PAGER ?
NO
YES
CHANGE OVER POWER SUPPLY CHANGE - OVER SWITCH 42
S4
POWER OFF PAGER UNIT 3 AND POWER OFF LINE TERMINAL UNIT 2
S5
POSITION REGISTRATION
S6
CHANGE TO TALKING MODE
S7
S8
INCOMING CALL TO PORTABLE TELEPHONE ?
NO
YES
TALKING
S9
TALKING IS FINISHED
S10

FIG.3

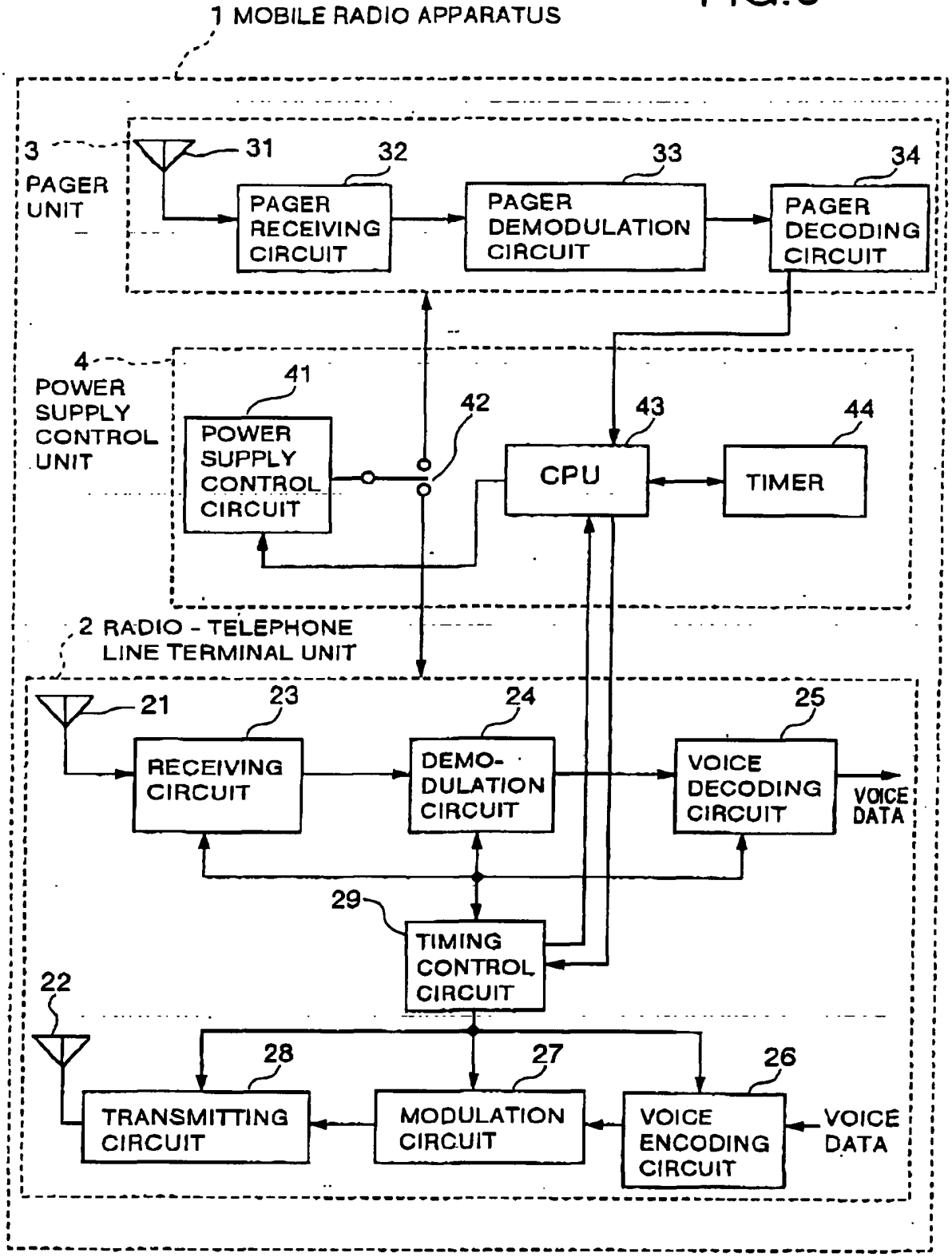

1 MOBILE RADIO APPARATUS
3
PAGER UNIT
31
32
33
34
PAGER RECEIVING CIRCUIT
PAGER DEMODULATION CIRCUIT
PAGER DECODING CIRCUIT
4
POWER SUPPLY CONTROL UNIT
41
42
43
44
POWER SUPPLY CONTROL CIRCUIT
CPU
TIMER
2 RADIO - TELEPHONE LINE TERMINAL UNIT
21
23
24
25
RECEIVING CIRCUIT
DEMO-DULATION CIRCUIT
VOICE DECODING CIRCUIT
VOICE DATA
29
TIMING CONTROL CIRCUIT
22
28
27
26
TRANSMITTING CIRCUIT
MODULATION CIRCUIT
VOICE ENCODING CIRCUIT
VOICE DATA

FIG.4

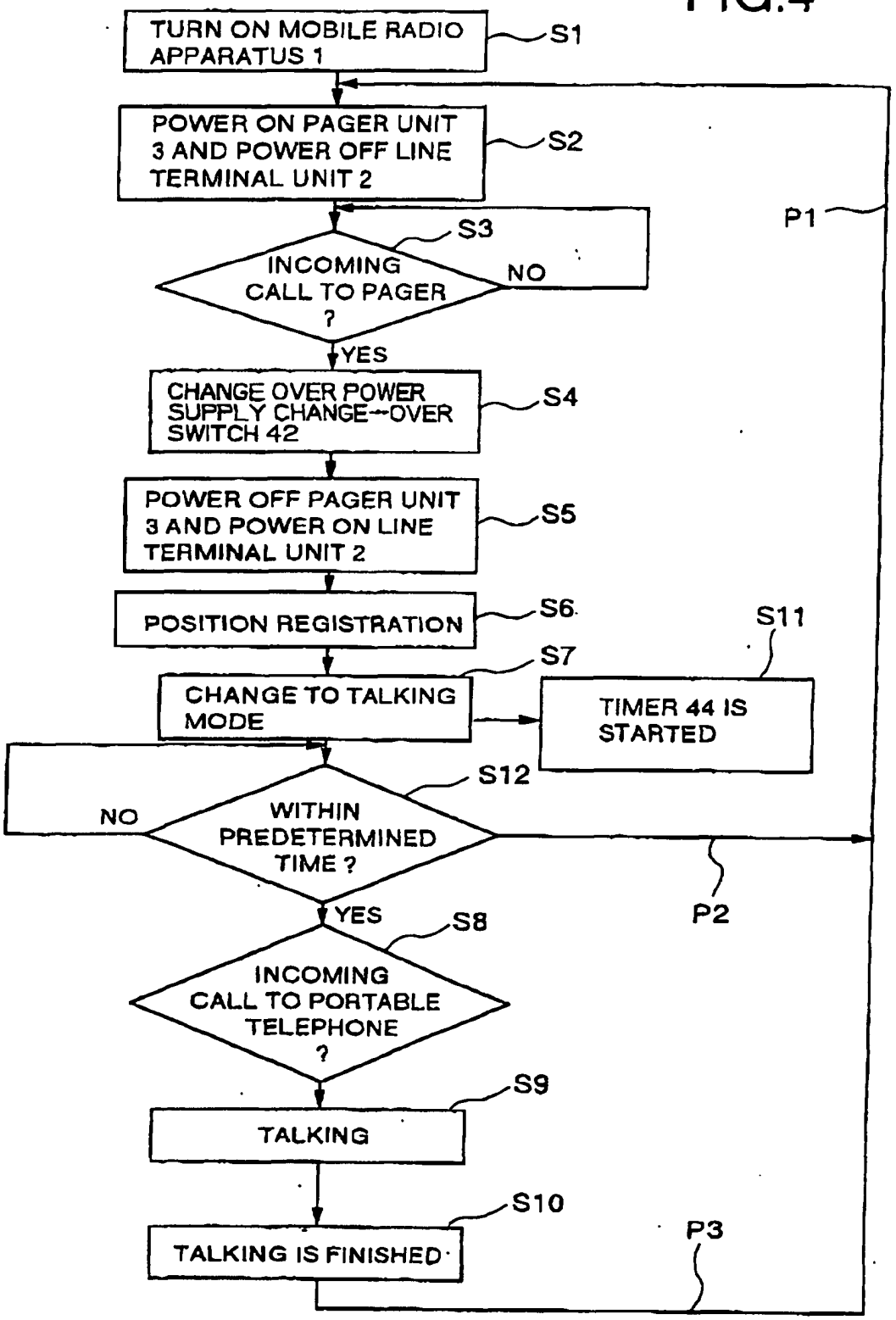

TURN ON MOBILE RADIO APPARATUS 1
S1
POWER ON PAGER UNIT 3 AND POWER OFF LINE TERMINAL UNIT 2
S2
P1
S3
INCOMING CALL TO PAGER ?
NO
YES
CHANGE OVER POWER SUPPLY CHANGE-OVER SWITCH 42
S4
POWER OFF PAGER UNIT 3 AND POWER ON LINE TERMINAL UNIT 2
S5
POSITION REGISTRATION
S6
S11
S7
CHANGE TO TALKING MODE
TIMER 44 IS STARTED
S12
NO
WITHIN PREDETERMINED TIME ?
P2
YES
S8
INCOMING CALL TO PORTABLE TELEPHONE ?
S9
TALKING
S10
TALKING IS FINISHED
P3

FIG.5

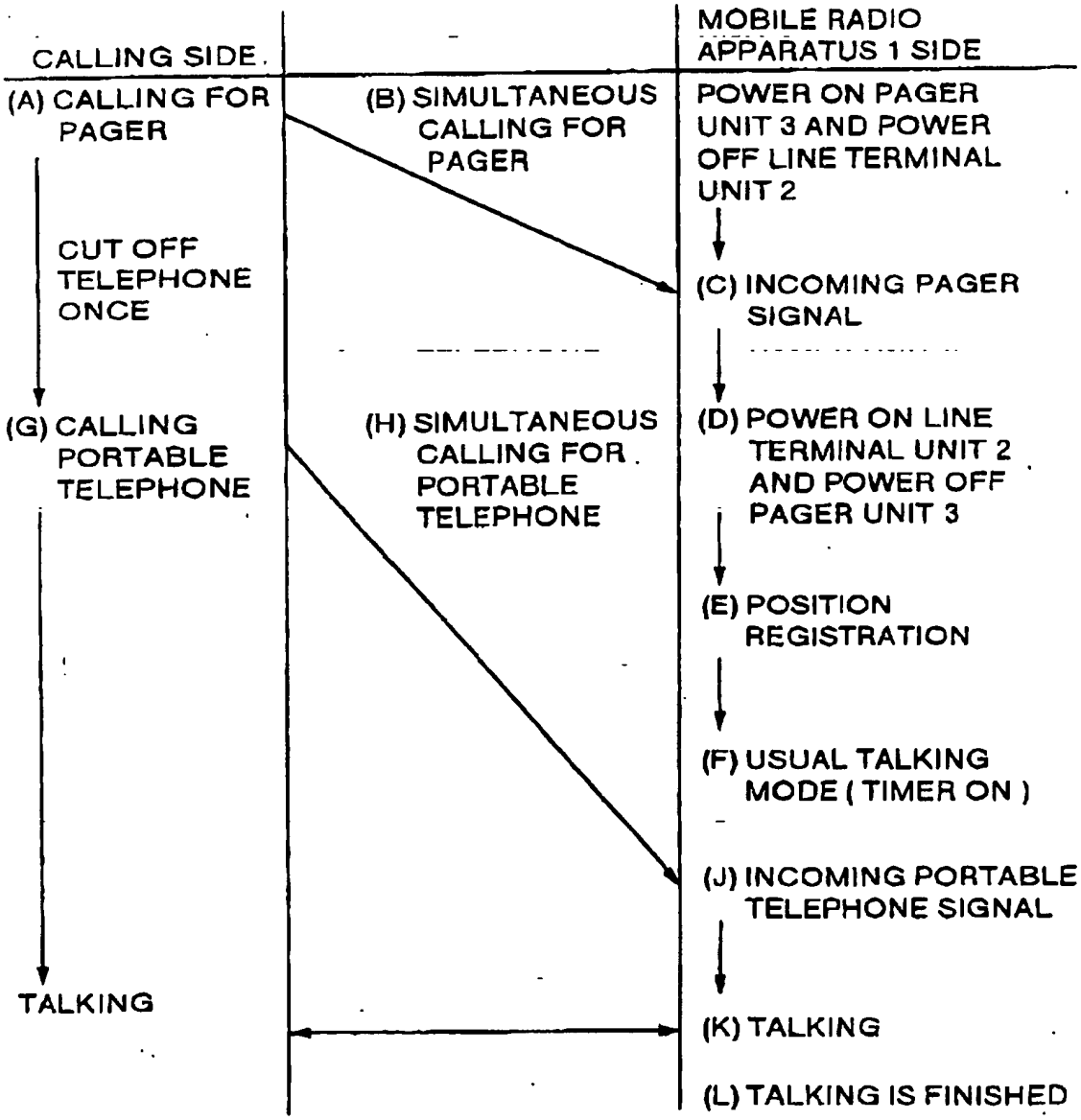

CALLING SIDE
MOBILE RADIO APPARATUS 1 SIDE
(A) CALLING FOR PAGER
(B) SIMULTANEOUS CALLING FOR PAGER
POWER ON PAGER UNIT 3 AND POWER OFF LINE TERMINAL UNIT 2
CUT OFF TELEPHONE ONCE
(C) INCOMING PAGER SIGNAL
(G) CALLING PORTABLE TELEPHONE
(H) SIMULTANEOUS CALLING FOR PORTABLE TELEPHONE
(D) POWER ON LINE TERMINAL UNIT 2 AND POWER OFF PAGER UNIT 3
(E) POSITION REGISTRATION
(F) USUAL TALKING MODE (TIMER ON)
(J) INCOMING PORTABLE TELEPHONE SIGNAL
TALKING
(K) TALKING
(L) TALKING IS FINISHED

FIG.6

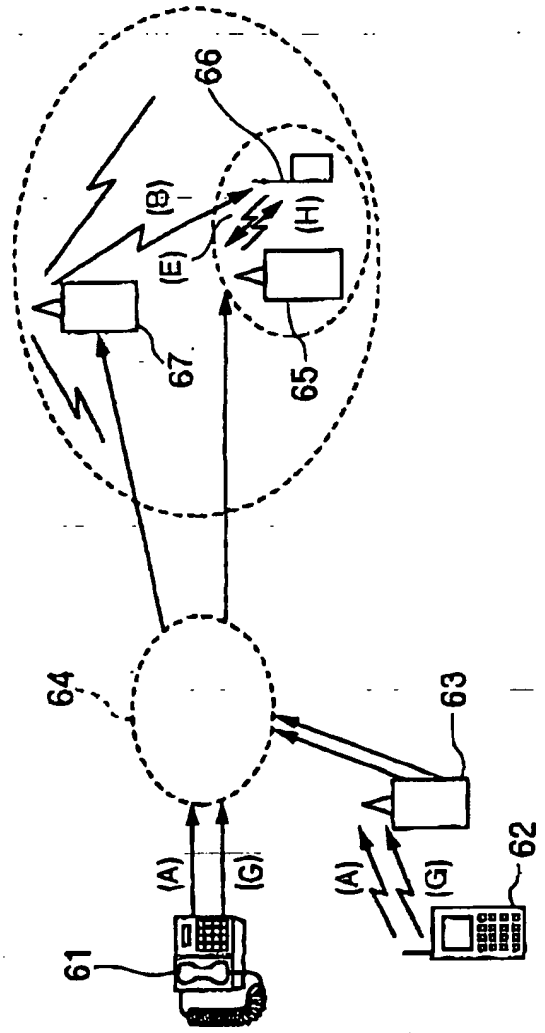
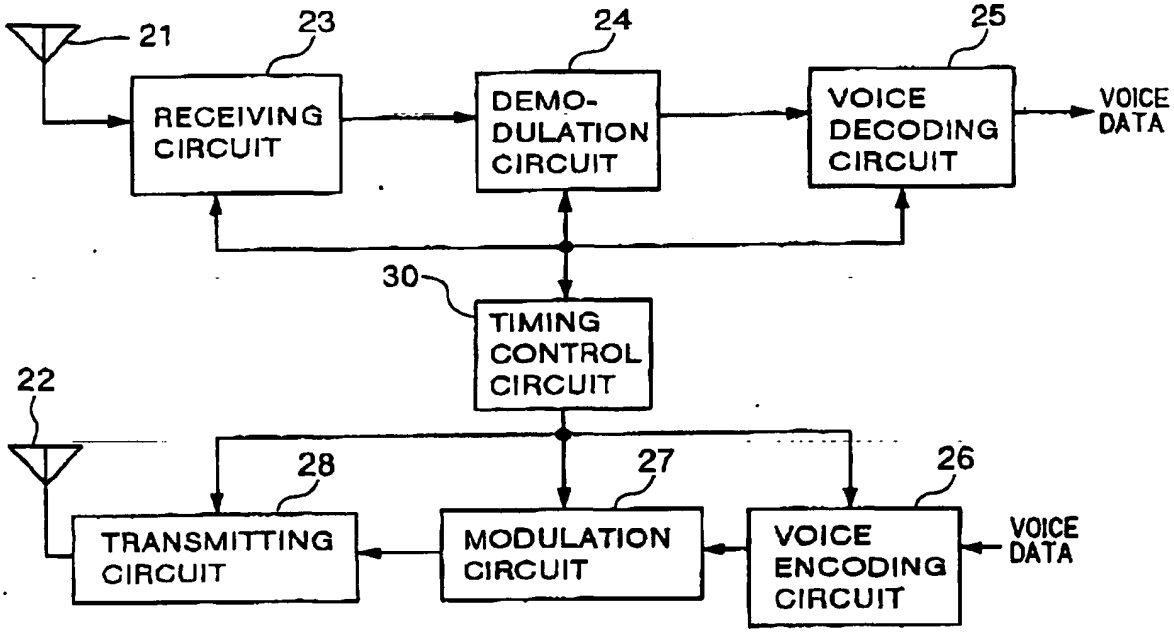


FIG.7 PRIOR ART



European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 93 30 9777

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.5)
A	GB-A-2 230 162 (MITSUBISHI) * page 5, line 17 - page 7, line 16 * * page 9, line 30 - page 10, line 15 *	1	H04Q7/04 H04B7/26
A	US-A-5 117 449 (METROKA ET AL) * column 2, line 10 - line 15 * * column 3, line 9 - line 30 * * column 3, line 66 - column 4, line 5 * * column 4, line 24 - line 62 *	1	
A	PATENT ABSTRACTS OF JAPAN vol. 16, no. 259 (E-1215)11 June 1992 & JP-A-04 057 592 (NIHON DENKI IDOU TSUUSHIN KK) 25 February 1992 * abstract *	1	

TECHNICAL FIELDS SEARCHED (Int.Cl.5)

H04Q
H04M
H04B

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	14 March 1994	Gerling, J-C

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
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E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

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EP 17230 (1)

PCT WORLD INTELLECTUAL PROPERTY ORGANIZATION
International Bureau

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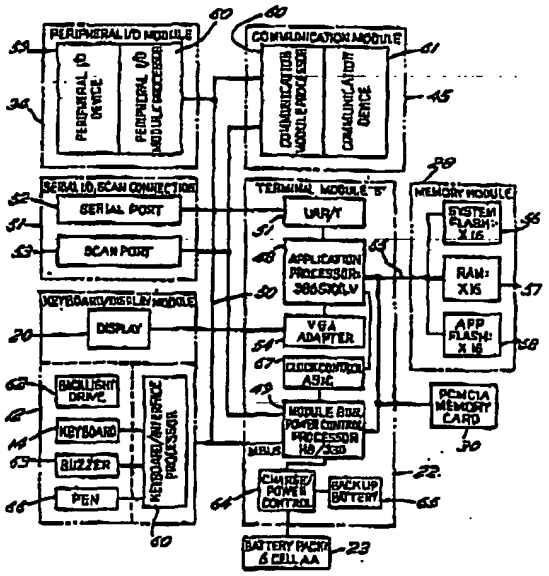
(54) Title: PORTABLE DATA PROCESSOR WHICH SELECTIVELY ACTIVATES AND DEACTIVATES INTERNAL MODULAR UNITS AND APPLICATION PROCESSOR TO CONSERVE POWER

(57) Abstract

A power management arrangement of a computerized portable data collection terminal includes a high speed data bus (50) which couples functional modules of the terminal via a plurality of microprocessor devices. The microprocessor devices interact to control selective activation of communication circuits to perform necessary communication or data processing functions and enter a power saving-dormant state during other times. Power savings are further realized from assigning control and monitoring functions to control processor (49) of a terminal module and data processing operations to high speed application microprocessor (48) with substantial computing power. Upon occurrence of an event requiring data processing operations, the application processor is activated, performs needed operations and is immediately deactivated to conserve power when not actively engaged in data processing functions. Typical data processing functions may include interpreting raw data from scanning operations, acting on keyboard inputs, performing data base operations and updating display screen information.



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PORTABLE DATA PROCESSOR WHICH SELECTIVELY ACTIVATES AND DEACTIVATES INTERNAL MODULAR UNITS AND APPLICATION PROCESSOR TO CONSERVE POWER

BACKGROUND OF THE INVENTION

This invention relates generally to portable data collection and data processing apparatus, and more particularly to microprocessor operated circuits for controlling the operation of such apparatus.

Portable, hand-held electronic data processing units have taken on an increasingly significant role in business control systems. Battery powered, hand-held data collection terminal units are used for inventory control in warehousing and merchandising operations. Other uses of such terminal units include invoicing, delivery route and order taking operations, and fast check-out and return control in automobile rental operations. Portable terminal units may typically include radio communications modules which maintain a real time communication link with a host computer and hence with a comprehensive business system.

Certain limitations affecting the use of these terminal units relate to communication route loading, namely to the limited number of terminal units which may conveniently become linked to a host over the same communication channel, or at best over a limited number of channels. Multiplexing and time slot access protocols typically establish upper limits for the number of data terminal units in any one system. To accommodate a larger number of terminals within any one system radio access becomes a premium. Data manipulation and compression prior to transmission and on-board data storage may be

implemented to increase data transmission rates and reduce access requirements. Typically, increased data processing capabilities are also accompanied by comparative increases in power consumption. In a hand-held, portable data collection and processing terminal an increased power consumption is, however, undesirable because of a resulting shorter operating cycle between battery recharge operations. Power saving improvements for such hand-held units are therefore highly desirable and are the subject of development effort.

Many diverse uses of hand-held terminal units or apparatus in present day business systems would ideally require a great number of distinct models of the terminals, each having a specific configuration tailored to one of the many particular uses. When changes in the hardware configurations of data collection terminals are implemented to meet specific needs, the manufacturing costs of the respective terminals tend to increase unreasonably. It has been attempted to reduce manufacturing costs due to model changes by providing functional modules which may selectively be used in distinct combinations to make up various models of a data collection and processing terminal apparatus. However, interconnecting modules in a number of different combinations tends to increase problems of communication among the selected modules. A particular problem relates to a decrease in product reliability when a great number of specialized data connections are needed. Simplification and further improvements are desirable to electrically couple in a simple manner any of a great number of combinations of functional modules for different models of portable data collection and processing terminal units.

Typically, the hand-held terminal units are controlled by microprocessor devices which operate

under the control of stored programs. Such devices are ideally suited for controlling various data processing operations. In general, microprocessor controlled operations of data terminal units involve data Input-Output (I/O) functions including displaying information on a screen, transmitting data messages by radio, receiving data inputs from data scanners or bar code readers and responding to keyboard inputs. Microprocessors also perform internal control functions such as monitoring power. Data processing operations or manipulations involve sorting, storing and retrieving both text and numerical data, as well as updating and controlling information in data bases. Popular data terminals also make use of various prompts and menus which may appear in a number of stacked levels. The speed of presenting updated menu information, requested data or other written instructions is considered a significant element in rating the performance of a data terminal unit. Although it is desirable to provide more powerful microprocessor functions to increase user friendliness by faster processing speeds, a resulting increase in power requirements for such more powerful microprocessors negates the feasibility of such improvements.

It is known in the art to use two or more microprocessor devices for more complex control operations. The processors typically operate in parallel, speeding up operations while maintaining comparatively lower clock speeds. Complex operations are thus completed at any given clocking rate in a relatively shorter time than with a single processor. A power increase due to an added microprocessor is offset by the greater computing power implemented without the need to drive a single microprocessor at a higher speed or to use a single microprocessor of a more complex architecture. However, portable data terminal units which require

extended operating time before having their power units recharged typically would not employ such multiple microprocessor enhancement.

To improve the usefulness of state-of-the-art portable, hand-held data collection terminal units, it would be desirable to implement further power saving circuit structures and operations and to provide interconnections among modules which are simple and reliable. Such improvements are seen as minimizing the cost of providing specialized configurations of data collection terminals, providing greater versatility and greater user friendliness.

SUMMARY OF THE INVENTION

It is therefore an object of the invention to provide a power efficient control circuit for a portable data collection terminal or data terminal unit.

A further object of the invention is to provide a reliable communication method and apparatus among various functional sub-units of the data collection terminal unit.

It is a particular object of the invention to provide for high speed serial communication among various functional sub-units of the data collection terminal unit.

Another object of the invention is to provide a control circuit which minimizes idle clocking cycles of power intensive microprocessor control and data processing elements.

A further object is to speed up response time to input, output and data display demands on a data terminal unit without a typical resultant increase in power consumption of such terminal unit.

In describing the invention, terms are given their typical meanings, the following definitions of which are believed to fall within these most commonly understood meanings. A microprocessor device is a control device capable of executing a sequence of logic instructions at a speed of operation determined by the frequency of clocking signals applied to the microprocessor. A memory or storage device may be a RAM (Random Access Memory), either volatile or nonvolatile, a ROM (Read Only Memory), or any of a number of available electrically programmable and erasable and otherwise permanent storage devices. Data are one or more numerical quantities or constants of predetermined value, representing individually or in combination intelligence or information. Data may be transferred over digital signal lines as binary signals, or as

radio frequency signals by RF transceiver units, or the data may be stored in storage cells, either temporarily or permanently, in typical storage devices or memories. A program is a sequence of logic instructions which, when applied to a microprocessor, control the operations of the microprocessor. An application program typically denotes a specific program consisting of a series of logic instructions which control the operations of a microprocessor in its manipulation, operation on, and routing of data by the microprocessor, as well as the generation of predetermined control signals or signal sequences at certain defined points in any operational cycle. The control signals may be applied according to selected program instructions to control, among other things, the terminal intelligence or operational sequences of the data terminal unit.

According to the invention, data communication and processing apparatus comprises a plurality of functional sub-units or modules. Selected ones of such modules include a communication and control device. A high speed data communication bus links the communication and control devices in each of the modules.

According to a more particular aspect of the invention the data communication and processing apparatus includes a base terminal unit which includes a first microprocessor element or device which is particularly dedicated to processing data. A selective activation of the data processing device or application device is controlled by the communication and control device of the base unit. The application element becomes deactivated during idle periods and its activation is initiated by the communication and control device upon receipt of a control signal indicative of the occurrence of an

event which requires data processing operations on data as a result of the event.

A more general aspect of the invention includes at least one communication and control processor device and a separate intermittently operable data processing element which is controlled by at least one communication and control processors.

Accordingly, a specific aspect of the invention includes an apparatus, including a microprocessor control circuit for use in data processing apparatus which includes a first microprocessor device which is dedicated to data processing operations. A second microprocessor device controls data input and output sequences of the data terminal unit and controls a selective application of processed data to or from the first microprocessor device to or from data output or input devices of the apparatus. The microprocessor control circuit is characterized in that the second microprocessor also controls the duty cycle of the first microprocessor device and in that the first microprocessor is operational for substantially less than fifty percent of an averaged period of operation of the control circuit.

--According to a particular combination the first microprocessor device may be a relatively more power intensive element, such as a 16 bit microprocessor and the second microprocessor device may be operational with relatively less power, such as an 8 bit microprocessor. The first and second microprocessor devices may be advantageously coupled to communicate through a parallel communications interface for transferring data between the two devices in response to interactive trigger or handshake signals. According to a particular feature of such combination, the first microprocessor device operates at least at twice the speed of the second microprocessor device and the second microprocessor device disables the first

microprocessor device after it has completed any particular operation and has communicated its completion to the second microprocessor device.

-- --Particular power saving features and advantages of such combination of the first and second microprocessor devices reside in the relatively less powerful device controlling and selectively turning on and off the more powerful first device which operates at a substantially higher clocking rate than the controlling second device. One of the advantages of the resulting intermittent operation of the first device is a power reduction with respect to a microprocessor control circuit having a continuously operational single device for providing a similar rate of screen updates, menu displays and data base manipulations.

Other features and advantages will become apparent from the following detailed description, which may be read in reference to the drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a schematic pictorial representation of a modular data collection terminal unit to which the present invention applies and showing schematically physical representation of modules of the data collection terminal.

FIG. 2 is a schematic diagram of functional interfaces among various modules of the data collection terminal shown in FIG. 1.

FIG. 3 is a schematic diagram of a control microprocessor, illustrating data bus terminals for synchronous communications.

FIG. 4 is a sequencing diagram showing schematically occurrences of a module-initiated communication sequence in accordance with features of the invention.

FIG. 5 is a further sequencing diagram illustrating schematically occurrences of a controller-initiated communication in accordance with features of the invention.

DETAILED DESCRIPTION OF THE INVENTION

Functional interconnections and power saving features of the present invention may be better understood from knowing how various building blocks or modules of a portable data collection terminal unit relate to each other. FIG. 1 shows a schematic arrangement of various physical modules or components that become integrated into the portable data terminal unit which is designated generally by the numeral 10. Hand-held terminals are of generally rectangular, elongate shape for accepted practical user friendliness, thus the modular terminal unit 10 desirably has an elongate, rectangular shape. An upper module 12 provides a sensory or physical interface to an operator of the terminal unit 10. The module 12 is referred to as a keyboard and display module 12 and features a keyboard 14 which may be a typical alphanumerical keyboard 14, including also function keys and cursor manipulation keys as part of an integrated keyboard arrangement. The keyboard 14 may be, and desirably is, a submodule 14 in itself, inserted and mounted into a mounting frame 15 of the keyboard and display module 12. In a typical manner, the depression of molded keytops 16 generally closes electrical contacts in a lower contact plane (not visible) of the keyboard 14. The type of keyboard 14 is, however, not critical and not considered limiting to the invention. The keyboard being a selected one of a number of available keyboards 14 is, however pertinent to the invention. For example, in one application the keyboard may be preferred to be a twenty or a twenty-four key keyboard 14. Such a keyboard 14 comprises comparatively few keytops 16 the locations and functions of which are more readily learned and accepted by an operator. Such keyboards typically do not have alphabetical key functions. Thus for many record keeping and

merchandising operations, the keyboard 14 having an array of twenty or twenty-four keytops may be most desirable. In another operation, a greater number of keytops 16 may be required to display the letters of the alphabet, numbers, and to provide keytops 16 for the execution of various functions. Thus, a keyboard 14 having an array of fifty-six keytops 16 may be preferred for example. Numerous variations in the arrangement of the keytops 16 within the array of the keyboard 14 are additionally possible. Mechanical or touch sensitive keytops 16 may be employed. In fact, touch sensitive keyboards which are known in the art, and which typically involve programming and bi-directional feedback, may be improved by interconnection features of the present invention which will become apparent from the detailed description as a whole.

The keyboard and display module 12 further includes an upper cavity 17 wherein a display screen 18 is disposed. The display screen 18 is preferably a state-of-the-art liquid crystal display, the liquid crystal display ("LCD") technology being well established in the art. "User friendliness" and versatility of the display ideally calls for a dot-addressable liquid crystal array screen 18 which permits the display of various alphanumeric characters and also permits the display of graphic symbols as well as display of Chinese or Japanese character symbols. Of course, dot-addressable graphic representations are known to require a substantial level of data processing and memory storage to permit the symbols to be displayed or moved about on the display screen 18 with reasonable speed. Long delays between the time that an operator pushes a keytop 16 to obtain data and the time that the requested data are displayed is considered "user unfriendly" and is commercially undesirable. A display technology which has become

a standard is referred to as VGA technology. VGA screens are capable of fine gray scale or color resolutions. The display screen 18 would be part of a selected display screen module 19 of a number of available display screen modules. FIG. 2 refers to a display screen module 20 which is similar in function, yet which may included selected differences to illustrate the advantages of the modular concept in combination with other features of the present invention. Display screens may vary in size or resolution or both, such that options among a number of display screen modules 19 may be made available to a potential user of the terminal unit 10. A display of an array of (128 by 240) pixels of, for example, (0.25 X 0.25) millimeter is an example of what is considered to be a desirable display screen resolution. Another screen array size may be (64 X 192) pixels, for example, of (0.35 X 0.50) millimeter per pixel.

The keyboard and display module 12 occupies most of the area of the terminal unit 10 which faces an operator when the terminal unit 10 is held and operationally used by the operator. Assembled to an underside 21 of the keyboard and display module 12 are preferably two major modules of the terminal unit 10. A first module is what is referred to as the terminal module 22. Whereas the keyboard and display module 12 is the major interface component between the operator and the terminal unit 10, the terminal module 22 is a major functional component of the terminal unit 10 itself, as will become apparent from the description herein. The terminal module 22 functionally controls the interaction of the various units or modules as described herein, and functionally is the control unit 22 of the terminal unit 10 as a whole. The terminal module 22 houses functional submodules and microprocessor circuits. A significant, and also space consuming

component is, of course, a power pack module 23. The power pack module may contain, for example six AA type rechargeable cells which may be arranged in a convenient flat arrangement and fitted into a battery end 24 of a housing 25 of the terminal module 22. The power pack module 23 supplies the power to various modules of the terminal unit 10, thus providing the capability for portable use of the terminal unit 10.

From the above description of potential choices of the type of display on the display screen 18, and further choices among keyboard arrangements of the keyboard 14, different requirements for electronic support circuits are indicated. One of the requirements in the support of changing functions economically is a means to provide a ready change in programmability of microprocessor circuits. Some module selections of the terminal unit 10 require less memory usage and different operational protocols than others. In accordance with a preferred embodiment, a memory module 27 may be selected as one of a number of differently programmed memory modules 27. However, in addition to being differently programmed, an alternate memory module 28, as shown in the functional diagram of FIG. 2, may include a different memory size (in cell numbers and in configuration). The terminal module 22 may further include an exchangeable memory card 30. The memory card 30 may be used to provide additional memory capacity as well as control programs for various desired functions of the various modules as described herein. The memory card 30 is schematically shown as being insertible laterally into a slot 32 of the housing 25 of the terminal module 22. However, the shown physical arrangement is but one of a number of equally desirable arrangements. Environmental protection of modules of the terminal unit 10 may desirably

suggest an enclosed and sealed arrangement for the memory card 30.

A peripheral I/O module 34 is shown in one of the two longitudinally opposite ends and is disclosed as being located at a lower or inner end 35 of the terminal unit 10. The inner end 35 is typically pointed toward an operator of the terminal unit 10, as the unit is held in the operator's hand with the keyboard and display module 12 directed upward toward the operator. The I/O (Input-Output) module 34 may typically include externally of a housing 36 a standard RS-232 and RS-485 connector 37. FIG. 1 also depicts a round communication connector 38. The peripheral I/O module 34 provides an interface between the terminal unit 10 and such diverse peripheral devices as "docks" which are batch transfer devices for accumulated data and battery charging devices, and cables which may connect to a code scanner, for example. The RS-232 interface may typically also become connected to a printer, for example. All these peripheral devices (not shown) are well known and are not part of the invention.

At a longitudinally opposite outer end 40 of the terminal unit 10, a serial I/O and scan connection module 41 may be attached. The scan connection module 41 is a high speed serial data communication module 41 which provides for serial data to be received in high volume from a scanner for example. Scanner data are typically received in a high density data string and require significant processing. As will become apparent from the further detailed description, a direct communication link to the data processing capability of the terminal unit 10 is provided through the scan connection module 41.

A further functional module of some significance is a communication module 44. Again in

reference to FIG. 1, the communication module 44 may be disposed adjacent the terminal module 22 toward the outer end 40 of the terminal unit 10. The communication module 44 is selected from a group of available communication modules of distinct functions. The selection of one of the communication modules such as the communication module 44 in FIG. 1, may characterize or classify the operation of the terminal unit 10. For example, a communication module 44 may have been selected from a group modules which include standard FM data radio transceiver modules, spread spectrum radio transceiver modules, modem communication modules, scanner device modules, or other data input devices. FIG. 2 shows a communication module 45 as an alternate to the physical representation of the communication module 44 shown in FIG. 1 to indicate a diversity of modules available for substitution. In further reference to FIG. 1, the communication module 44 is shown as having an antenna 46, indicating the selection being a transceiver unit for radio frequency real time communication with a data system. Such a data system includes typically a further transceiver station, not shown, with which the transceiver module 44 communicates. The second transceiver station as a receiving end of a link is not shown as it is commonly understood that communication is the transfer, the transmission or reception, of information or data over a communication link established between two points. The operator of the terminal unit 10 also constitutes a second end of a communication link that is established by the operator's manipulation of the keyboard 14 and by the operator's visual perception and recognition of the data displayed on the display screen 18. Thus, the term "communication" is understood as linking the modules to other units. The presence or absence of the

other units is of little significance to the teachings of the present invention. These external units are therefore not shown to better emphasize the features of the invention.

Referring now to FIG. 2, there is shown a functional schematic diagram of a combination of the physical modules discussed with respect to FIG. 1 or of alternate equivalents of the modules in FIG. 1. The modules with respect to which preferred physical positioning was discussed in reference to FIG. 1 are now shown functionally related in FIG. 2. The terminal module 22 clearly appears as a central functional device. It is to be noted that the schematic representation refers to functional or communication rather than electrical connections. The power pack 23 is typically coupled to power all electrically driven circuits of the terminal unit 10. The power pack 23 is functionally and physically coupled to the terminal module 22. While electrical power is distributed from the power pack 23 to all electrically powered or controlled modules of the terminal unit, the remaining power of the power pack is actually monitored by a function of the terminal module 22. The power pack 23 as the sole portable power source for the terminal unit 10 would, but for power saving provisions, experience a significant power drain during the operation of the terminal unit 10.

Power savings are implemented in a manner which typically implies a greater usage of power but which enables power savings by more selectively using circuit functions as they are needed. Accordingly, the terminal module includes preferably first and second microprocessors 48 and 49, respectively. The first microprocessor 48 is a data processing device and is also referred to herein as an application processor 48. The application processor may be any of a number of available microprocessors available.

Desirably the application microprocessor 48 has the capability of processing data with greater word length or word width than the second processor 49. The term word width refers to the number of data bits that are capable of simultaneously being processed, retrieved or stored. The application processor 48 is therefore one capable, for example, of processing a 16-bit or a 32-bit data word. The processing speed and clocking rate would desirably exceed those of the second microprocessor 49. At present, the more powerful microprocessor, such as the microprocessor 48, also has a higher power requirement than the second microprocessor 49. However, even with the high power requirement during operation, power savings may be achieved by providing a rest state at which the microprocessor 48 is, for example, not clocked and thus deactivated.

The second microprocessor 49 is also referred to as a control processor 49. The second microprocessor controls the operation of the terminal module 22 and controls communication within the terminal module as well as among the various other modules of the terminal unit 10. Desirably, the control processor 49 does not have the operational power requirement as the application processor 48 for reasons that will become apparent. Control is an ongoing function. Although the operational speed of the control processor 49 is comparatively slow with respect to that of the application processor 48, the operational power consumption of the control processor 49 is also desirably lower than that of the application processor 48.

A presently preferred device for the control processor is of the characteristics that are presently found in a Hitachi H8/330 type microprocessor device. The Hitachi H8/330 processor

features on-board memory which is convenient for its intended operation as will be seen in reference to its operational modes as set forth herein. The H8 type processor is an 8-bit processor, capable of processing data in an 8-bit word length. However, the control processor need not be an 8-bit processor. In general, the word width processing capacity of the control processor 49 would be chosen to be relatively less than that of the application processor 48. The control processor 49 does not require the processing speed that is desirable for the application processor 48, and, according to the state of the art, processors with relatively low word width processing capacity (considering processors in general) require less processing power. It is to be understood, however, that the specification of any particular device, such as was done with the Hitachi H8-type microprocessor for the control processor 49, is for illustrative purposes only. Continual development efforts in microprocessor architecture is expected to result in various commercially available devices that may be of equal or better utility than the specified exemplary devices. The features and desired functions of the invention will be helpful to one skilled in the art to select any of a number of acceptable devices to function in the desired manner as described herein.

FIG. 3 shows a schematic block representative of signal terminals of the control microprocessor 49 which are pertinent to the preferred mode of implementing the present invention. In describing the significant signal and data terminals, a bar above a designation indicates a signal low being the active state of the signal. In the specification hereof the inverse or signal low active state is described with an "N" preceding the letter name at the respective signal term.

To communicate among the various described modules, four signal leads of the control processor 49 define the leads of a communication bus 50 referred to herein as "MBUS". The MBUS 50 is a high speed synchronous serial data signal bus which may, and preferably does, operate at a signal rate of 500 kilo bits per second. Better reliability of data transfer is achieved by using the high speed data bus. In a modular structure in which the modules are readily uncoupled and reconnected to permit convenient changes during the manufacture of the final product of the terminal unit 10, the reliability may be noticeably affected by interconnection faults. When reliability decreases with each additionally coupled module, the advantages of modular structure are quickly dissipated. In contrast to typical parallel data buses used to link components of electronic products or systems, the present system architecture of the modular terminal unit 10 significantly reduces the number of contacts needed to interconnect the various modules.

Reliability might be further decreased by electrical noise and interference coupled into the interconnected signal lines. With fewer signal lines to manage, it becomes feasible to protect each line from noise and interference effects by using well known shielding, impedance reduction and termination techniques. Thus, the system of the present invention provides greater reliability than modular systems with conventional parallel data transfer.

FIG. 3 shows a four signal terminal which constitutes the MBUS concept. "MCLK" is the clocking signal which synchronizes the modular counterparts of the control processor 49. The clocking signal provides for a bit rate of 500 kilo bits per second. The terminal labeled "MTXD"

transfers data from the control processor onto the MBUS 50. The terminal labeled MRXD receives data from other modules over the MBUS 50. The low signal active "NMATT" is a control signal line which indicates that data will be communicated over the MBUS 50. These four lines effectively permit the various modules to communicate among each other.

A number of signal contention protocols are available and are commonly known for resolving potential collisions in data communication. Any of the various contention protocols will suffice to resolve priority conflicts when data are to be transferred among the various modules. It is to be understood that any standard conflict resolution procedure also may be modified if so desired to assign specific priorities for communication among the modules. For example, data received from a scanning operation may be accepted and processed on a priority basis. Keystroke inputs from the keyboard and display module 12 may be given priority over data flow from the communication module 45. Similarly data messages received via radio transmission from an external master unit (not shown) may be given priority. Program altering instructions may be embedded within a data message. The embedded instructions may affect future operations that are about to be received from one of the modules.

Further with respect to FIG. 3, corresponding data lines interfacing with the application processor 48 are indicated as parallel signal lines DB0-7 and data lines A0-3. Data communication and control procedures between the control microprocessor 49 and the application processor 48 are further described with respect to alternate embodiments.

The application processor 48 is coupled to an asynchronous device or "UAR/T" function 51 with an

output coupled to a serial port 52 of the serial I/O scan connection module 41. The serial I/O scan connection module 41 further includes a scan port 53 which links to the control processor 49 and enables it to communicate control signals, such as, for example, scan trigger signals. The application processor 48 is further coupled to a VGA adapter circuit or driver 54 for driving the display screen 20. The display screen function is processor intensive. Data processing operations are, therefore, managed directly through the application processor 48. The data processing operations performed by the application processor 48 are in most instances memory-usage intensive. Consequently, the application processor 48 is linked by a conventional data bus 55 directly to the memory module 28. The memory module 28 is shown as including representative data storage functions or circuits including a 16-bit word width system FLASH-programmable memory 56, a typical 16-bit word width random access memory 57 ("RAM"), and additional application FLASH-programmable memory 58, also preferably 16-bit word width. The 16-bit word width storage devices or functions 56, 57 and 58 are preferred in conjunction with a 16-bit microprocessor device representing the application processor 48. Presently preferred devices may be for example a Chips and Technologies F8680 device or an Advanced Micro Devices 386SXLV processor. It must be understood, however, that other devices may exist or may become available that are equally acceptable or even better suited to function as the application processor 48. In addition, selecting a different microprocessor 48 may result in a different selection of memory device types, word widths, or storage capacitites.

The peripheral I/O module 34 may, as discussed with respect to FIG. 1, include standard connectors

for coupling the module 34 to an external device. A particular device 59 may be a portable printer device, as shown in the function block 59 of FIG. 2, which may be mounted or coupled directly to the terminal unit 10. The peripheral I/O device, whether it is a printer, a reader, or other data input or output device, would functionally include a microprocessor 60. The microprocessor 60 is chosen to interact with the MBUS system and is coupled in each described element to function as a terminal element, i.e., an interface communicatively coupling the respective logic circuits of the module to the MBUS. Thus, when the respective microprocessor receives a communication over the MBUS 50, a recognition of control codes may cause the microprocessor 60 to transfer data or execute a control instruction, which may entail activating or de-activating the power circuits of the respective module or conditioning the module to receive or transmit data.

The communication module 45, which, for example, may be a modem or any of a number of available radio frequency transceiver modules, also includes a compatible microprocessor 60 which interfaces with a respective communication device 61 of the module 45. The communication device 61 would, corresponding to the desired function of the module, be a modem or transceiver device, for example. To be compatible with the MBUS data format of the other described modules, the keyboard and display module also preferably includes a distinct interfacing microprocessor device 60. The keyboard and display microprocessor 60 is coupled to control various elements which are directly associated with the keyboard and display module 12. A particular function that may be conveniently controlled via the MBUS 50 and the respective control processors 49 and 60 is a backlight drive 62 function for the display

screen 20. Another function incorporates a buzzer 63. The buzzer 63 may be programmed to signal an audible alarm as a response to an incorrect key depression by an operator. The buzzer 63 may further be used to alert an operator when a charge and power control circuit 64 detects that the power pack 23 has become discharged and a backup battery 65 is being engaged. In addition, the power control 64 may function to shut down the terminal unit 10 from further operation until the power pack has been recharged or replaced. In the preferred mode, power from the back-up battery 65 would nevertheless be maintained on the control processor to enable it to determine when the power pack 23 has in fact been recharged or replaced.

The processor 60 of the keyboard and display module 12 may also control other input or output devices that may be coupled to the keyboard and display module 12. For example, a pen 66 may be coupled to the keyboard and display module 12 for use in connection with a pen stylus sensitive keyboard module 14, or in connection with a pen stylus sensitive display screen 20. In this latter instance, the display screen module 20 becomes an input device in addition to being an output device. The input is received through manipulation of the pen 66 by an operator.

The application processor 48 and the control processor 49 are preferably controlled through a timing Application Specific Integrated Circuit 67 ("clock control ASIC"). The clock control circuit 67 may be driven from a single clock signal which is then divided to provide respectively different clocking rates to each of the processors 48 and 49. The implementation of the timing circuit 67 in a single circuit function is more efficient and provides synchronization among the components and

modules. A second clock signal for implementing a real time clock may be provided.

In addition to the reliability advantages of coupling modules via the four-line MBUS mentioned above, the MBUS 50 also provides a space saving advantage, i.e., more compact physical routing of cables among the modules.

Power savings which are obtained through the control of the functions of the various described modules via the MBUS 50 will be best understood from the following description in reference to FIGS. 4 and 5. To conserve power and prolong the operational time of the terminal unit 10 between recharges or replacement of the power pack 23, the control processor 49 and the related MBUS module processors 60 perform a special power-saving control function: any module which is not in active use is placed into a dormant state.

The MBUS 50 communicatively interconnects the modules of the terminal unit 10, such as the peripheral I/O module 34, the communication module 45, the keyboard and display module 12 and the terminal module 22. Other modules which in the future may be included in the active communication network of the MBUS 50 may simply be added as described herein. For each module, one of the microprocessors 60, having the data terminals of the microprocessor 49 shown in FIG. 3 (i.e., terminals MCLK, MTXD, MRXD and NMATT) is coupled to the respective lines of the MBUS 50 to become part of the internal communication network of the terminal unit 10. The microprocessors 49 and 60 constitute the terminal elements of the communication network represented by the MBUS 50. For each module, the respective microprocessor 60, though it may be physically identical to the control microprocessor 49, functions as a subservient processor to the control processor 49. The microprocessors 60

become a communication interface between the MBUS 50 and the functional circuits of the respective module, whether it is the communication module 45, the keyboard and display module 12 or the peripheral I/O module 34. Inputs from the respective module are accepted by the processor 60. An H8/330 microprocessor includes internal memory for receiving and temporarily storing data communications. Programmable ROM on the H8/330 permit instructions to be stored which particularly configure the microprocessor as a module processor 60. The interface operation of the microprocessor 60 differs from the controlling operation of the control processor 49 as may be realized from the description of the interaction of the processors in reference to FIGS. 4 and 5.

A normal state of the microprocessors 49 and 60 is a sub-active or dormant state. In this state, the module processors 60 and the control processor 49 are clocked at a power saving "slow" clocking speed. The sub-active or dormant operational state permits the module processors 60 and the control processor 49 to execute certain long-interval control functions, such as watching for a keytop depression by the keyboard and display screen processor 60 or a low battery signal to be received by the control processor 49 from the charge and power control circuit 64. Upon occurrence of an event which affects the operation of any typical communication function which is driven over the MBUS 50, all modules and the control processor are placed into a fully activated mode. The control processor 49 queries, directs and controls communication over the MBUS 50.

For example, FIG. 4 shows an activation cycle of the MBUS 50 which is initiated by one of the described modules other than the terminal module 22, i.e., from one of the processors 60. The respective

processor 60 drives the NMATT line of the MBUS 50 into a low signal state. The low state of the NMATT line activates all processors 60 to receive an inquiry or instructions. At T1 in FIG. 4, all modules have been placed into the active state. During the time interval T1 to T2 the control processor sends a query or polls the activated modules over the MTXD line, which is reserved for transmissions originating from the terminal module 22, i.e., from the control processor 49. The query would typically contain at least one byte of data. The quantitative translation of the byte of data indicating to the processors 60 that it is a query in response to one of the module processors 60 having driven the NMATT line to a low state. The query shown at 71 signals the processor 60 to transmit its data message over the MRXD line of the MBUS 50. At the onset of the data transmission 72 from the respective communicating module processor 60, the NMATT line is restored to a high state, placing all other modules back into the dormant condition. As shown in FIG. 4, the data communication may proceed for a variable length-of time past the time state T2 at which the NMATT line has returned to a high state. Upon termination of data communication from the respective module processor 60 to the control processor 49 the control processor 49 sends a message 73 confirming correct receipt of the data message (at T3). Again the confirming data message contains at least one byte of information, the decoding of which would either indicate an error code or signal the correct receipt of the data message. At that time (at T3), the communicating module processor 60 and the control processor 49 also assume the power saving dormant state.

FIG. 5 describes a very similar event in which the control processor 49 drives the NMATT line to a

low state. Again, all processors 60 assume an active state and receive a communication 75 of typically at least one byte of information from the control processor 49 during the time interval between T1 and T2. The information 75 contains an address of the module to which a data message from the control processor 49 will be directed. The respective module processor acknowledges its understanding of the address by a responding message 76 which may be translated by the control processor 49. In response to the receipt of the message, the control processor releases the NMATT line which assumes its normal high state and places all non-affected module processors 60 again into a dormant state. The control processor 49 then transmits its data message as indicated at 77 to the respective previously addressed module processor 60. At the conclusion of the communication 77 from the control processor 49, the respective module processor acknowledges receipt of the communication 77 by its response 78. On transmission and interpretation of the response 78 that the communication 77 has been received correctly, both the control processor 49 and the respective module processor 60 assume their dormant states. It is to be noted that the respective data messages shown in FIGS. 4 and 5 indicate durations of data messages. It is to be understood that the high and low states of other than the NMATT line indicate a time interval during which a great number of high or low states in synchronous time slots are transmitted essentially at the bit rate of 500 kilo bits per second. This bit rate may include start and stop intervals.

In the described communication events, power consumption by the terminal unit 10 is minimized by providing for a quasi dormant state for substantially all functions of the various modules, such that electrical power is used in pulses during

the described query states and only in spurts by certain modules during real time performances. Highly power intensive data processing operations in the terminal module 22 provide further power savings in communication from and to the various modules.

The term "data processing operation" is used herein to describe the manipulation of a series of binary codes according to programmed instructions to arrive at a desired result. Because of the great number of discrete binary operations required to perform many of the most common data processing functions, higher processor speeds and more complex or powerful microprocessor circuits of those typically available are more desirable for data processing operations.

The application processor or data processing device 48 may be an "Intel 80C188EB" device which is "16-Bit" microprocessor device, operated at a preferred speed of 9.2 megahertz (MHz). At such preferred clocking speed of 9.2 MHz, the power consumption or operating current consumed by the data processing microprocessor device 48 is approximately 55 milliamps ("mA"). The control processor 49 is in the particular implementation a "Hitachi H8/325" device which is an "8-Bit" microprocessor, operated at a speed of one-half of the speed of the data processing microprocessor 48, or 4.6 MHz. Because of the smaller physical size of the control processor 49 and the slower, preferred clocking speed, the power consumption or current required by the control processor 49 in its operational mode is only about 9 mA, hence less than one-fifth of the power consumed by the processor 48. Because of continuous advances in the field of microprocessors over the past decade, it is to be expected that in the future other microprocessors will be marketed which will meet or exceed the requirements of the presently preferred

microprocessors and that these microprocessors also may operate in accordance herewith. In general, the control microprocessor circuit or the control microprocessor 49 desirably operates at a slower and less power consuming speed than the application microprocessor circuit or the application microprocessor 48. A one-to-two speed ratio for driving the respective microprocessors 49 and 48 is preferably chosen because of the power savings that are realized with respect to the portable terminal unit 10.

The clock control circuit 67 may be expanded in its function to include an interface circuit between the processors 48 and 49, which incorporates data transfer as well as clocking functions. The clock control circuit 67 would include in such coupling arrangement a typical divide-by-two timing circuit function. An original 9.2 MHz clocking signal port and a signal port with the divided by two signal would be coupled to the respective timing signal input ports of the processors 48 and 49, respectively, to drive the processors 48 and 49 at their respective speeds of 9.2 and 4.6 MHz. As already described, a second clock may be coupled to the clock control circuit 67 to provide a real time clock.

The preferred control processor 49 includes in its commercial implementation, in addition to typical microprocessor registers and an arithmetic logic unit, such functional circuit blocks as ROM, RAM and communications ports. According to a preferred embodiment, data communication between the processors 48 and 49 occurs via an interface circuit including, for example, two 8-bit data registers or latches (not shown). It is to be understood, however, that the control processor 49 may have a direct bus interface provision and become directly coupled to the application processor 48, the coupled

processors 48 and 49 thereby being capable of bidirectionally passing data and control signals without two 8-bit data registers or latches. Also, data latches are generally considered temporary data storage devices. Data from one device are latched into a respective data latch to be retrieved by a second device. Therefore, in general, the operation of the data latches constitutes a primitive equivalent of what is known as a dual port memory. Dual port memories or memories which are accessed via at least two ports are known in the art. The substitution of the below described latches with a dual port memory in a "data storing interface" is therefore considered to be within the scope of the present invention. The clock control ASIC function 67 shown in FIG. 2 should be understood to not only include the clocking signal coupling circuits to drive the respective application processor 48 and the control processor 49, but to further include the data interface or bus to permit the desired bidirectional data and control code communication between the processors 48 and 49 as further described herein. In further reference to FIG. 2, an integration of the processor devices 48 and 49 into a single device desirably may include the referred to function of the interface and clock control circuit 67 as an integral part of an integrated circuit (not shown).

Tests have shown that typical data processing operations performed by the application processor 48 require approximately 10 milliseconds of time, and not more than 20 milliseconds, on the average. It has further been found that a more user friendly and a more practical response time may be obtained from the terminal unit 10 with less power required when substantially all data processing operations are performed by the application processor 48 and the application processor is subsequently immediately

deactivated, than if a single alternative microprocessor circuit were used operating at a higher rate and including sufficient computing capacity to perform all required functions in an appropriately short time. In the preferred selection of the two processors, the combination of the application processor 48 and the control processor 49 amounts only to an approximate increase in current usage of typically about ten percent, and in the extreme, of no more than 20 percent over the normal operating current level of the control processor by itself. The combined power consumption of the application processor 48, as controlled by the control processor 49, and the control processor 49 is about one fifth of the power consumption of the application processor 48 itself when it is operated continuously. However, the display speed and data manipulation speed of the terminal unit 10 essentially is the same as if the terminal unit 10 were controlled by the more powerful application processor 48.

The operating current requirement for the application processor 48 is directly related to the number of actively switching elements in each computational operation. Though having an interrupt function, the referred to 80C188EB processor 48 does not include, in contrast to the control processor 49, any internal memory devices. FIG. 2 consequently shows a data bus 55 of the processor 48 coupled to external memory devices, such as the system FLASH memory 56 (functionally equivalent to a read-only memory or "ROM"), the flash electrically erasable and programmable read-only memory 58 ("FLASH EPROM") and a typical random access memory 57 ("RAM"). The data bus 55 further couples the application processor directly to the display module 20 ("LCD DISPLAY") of the terminal unit 10, such as a dot addressable LCD graphic screen module, for

example. A direct data transfer by the high speed application processor 48 to the LCD screen is preferred because of substantial amounts of data handling or processing that is required in updating a particular screen. For example, even a small graphic screen display, such as a screen of 48X100 pixels, requires that each of the pixels be updated on a continuous basis. Typically, control circuits, which are part of the data display function of the module 20 and are not separately shown, and which may be specific to a particular screen display, may routinely re-apply currently displayed information dots in a cyclic refresh operation to the already identified pixels of the screen. However, to update the screen, each pixel of the screen must be updated. This is so for any updating of the screen, even for a simple display line scrolling operation which an operator may not even consider noticeable or significant. To facilitate such updating of information in a prompt, user-friendly, and power efficient manner, a data processing operation and the high speed passing of the updated data between the RAM memory 57 and the data display 20 is performed during a short operational activation of the application processor 48. More data processing with respect to the data display screen 20 may be required for routine menu operations. Menu operations are particularly desirable for such portable terminal units 10 because the typical user may not be well acquainted with computer terminals. Well defined menu operations with a number of available menu levels are found to significantly increase the user friendliness of a terminal unit. An efficient menu operation is known to involve data base searching and data retrieval in addition to the normal display screen updating operation. The described microprocessor circuit with the selectively activated data processing device 48 and

the relatively smaller and slower control processor 49 has been found to be particularly advantageous for these purposes.

A selective activation and deactivation of the microprocessor circuit portion implemented by the data processing device or application processor 48 would also provide power savings when the operating speeds of the two processors 48 and 49 are the same. If both processors 48 and 49 are being operated at the same speed, however, the power savings is not as great as that realized in accordance with the preferred embodiment of the described invention.

FIG. 2 shows schematically an arrangement of electrical components of an exemplary terminal unit 10, and of the preferred interactive relationship of such components with the application processor 48 or the control processor 49. In the embodiment shown in FIG 2, the application processor 48 controls directly the RS-232/485 standards serial interface 34. The flash EPROM programmable read-only memory 58 is preferred to have no less than 256K byte storage capacity. The flash EPROM may supplement or even replace standard ROM, such as memory 56 which is preferred to have at least a 512K byte storage capacity. In the preferred example of the terminal unit 10, the ROM, if used, would provide typical and normally non-variable data processing protocol instructions. Such ROM may include control instructions for standard display updating routines as well as for other routines which are typically implemented by standard keyboard instructions and which pertain to typical data input and output commands.

The random access memory 56 is in the specific embodiment a semi-permanent static RAM type circuit. The memory may have a capacity of 512K bytes. The preferred data storage capacity has been determined to provide sufficient storage for an on-board data

base related to typical inventory or delivery route type information. In view of the portability of the terminal unit 10, an unexpected loss of battery power may bring about a significant loss of information unless the data stored at the time of a temporary loss of battery power are protected from destruction until full battery power is restored. For example, the terminal unit 10 may be returned at an initial signal of "low battery" to a battery charger unit (not shown) for a recharging operation and any stored data may be transferred, even while the battery 23 is being recharged, from the terminal unit 10 to a host computer (not 16 shown in FIG. 1).

A preferred LCD display 20 is a graphic display having an array of 48 x 100 pixels. Typical menu or special graphic screen data may be pre-established for a particular terminal unit 10 or for an application group of such units and may be stored initially in the specific ROM 56 provided for the particular unit or units 10. As previously discussed, the updating of displayed data on the screen device 20 requires a significant amount of data processing. Typically, such data processing operations involve accessing permanently stored screen display information, such as from the ROM 56 or from the flash EPROM 58, the manipulation of such information, and temporary storage of such manipulated information in the random access memory 57. As shown in FIG. 2, the application processor 48 has direct functional control over the respective devices for such data updating manipulations with respect to the LCD Display screen 20.

Another function that is desirable in connection with LCD display screen 20 is contrast control. In regards to FIG. 2, such a control may be integrally coupled to the VGA adapter circuit 54. The contrast of the LCD display screen 20 is typically set and adjusted by an operator and is a

matter of choice. The contrast may be adjusted for example by a typical key depression or by a keyboard sequence given by an operator. Such control input executions are within the scope of operations of the control processor 49. The contrast display may be controlled as indicated in FIG. 2 by the functional coupling of the keyboard circuit 12 to the control processor 49 and the further coupling of the processor 48 to the contrast control circuit and then directly to the LCD display screen circuit 20.

The LCD display screen 20 in the preferred embodiment is equipped with the back lighting drive 62. Many warehouse operations, route delivery operations and even merchandising inventory operations must often be performed under sufficiently poor lighting conditions, thereby requiring a backlighting source to be supplied as a standard feature of the LCD display screen 20. A preferred backlight drive circuit 62 is preferably coupled through the MBUS 50 to the control processor 49. A preferred backlight drive circuit for use in conjunction with the exemplary terminal unit 10 is described in applicant's co-pending PCT patent application Serial No. PCT/US9208646 filed October 12, 1992. Because an operator may wish to adjust the backlighting (i.e., for example, its brightness or luminescence), both the application processor 48 and the control processor 49 may interact with the backlight drive circuit 62 to provide for an operator controlled brightness control sequence to be communicated to the backlight drive 62.

Besides the timing function circuits for the real time clock and its functions, the control circuit 67, as an ASIC, may also include the clocking signals to each of the two processors 48 and 49. The control circuit 67 may also provide the data communication functions between the application processor 48 and the control processor 49 by two

latching circuits as mentioned above. Also as mentioned above, the control processor 49 functions to activate or "wake up" the application processor 48 for data processing operations. In one contemplated embodiment the control circuit 67 may include integrally a switching circuit function for separately switching the application processor 48 off or on. Such a switching operation may be implemented by a typical switch as part of the integrated control circuit 67 which selectively interrupts and reestablishes the clocking signal to the application processor 48. The function of deactivating and reactivating the application processor is controlled in a preferred embodiment via the control device 67 in a somewhat different manner. Instead of controlling the clocking circuit to the application processor 48 in the control circuit 67 with a control signal from the control processor 49, the control function is preferably split. In other words, the application processor 48 provides a shutdown status signal to the control processor 49 and then shuts itself down. The control processor 49 subsequently returns the application processor 48 to an active state upon the occurrence of any event which requires the operation of the application processor 48.

Further in reference to FIG. 2, a trigger control signal of the scanner module 41 may be received by the control processor 49. However the data flow from the scanner module 41 would be received directly by the application processor 48 for further processing and storage. Input signals which are received at speeds within the operational capability of the control processor 49 are received by and transferred through the control processor 49. For example, key depression signals from the keyboard 49 are preferably received directly by the control processor 49. A preferred keyboard size for

the terminal unit 10 referenced herein, as indicated in FIG. 2, is a 6x8 key matrix. Such a size is optimal because of space considerations and requires that multiple functions be implemented by each of the keys. However, the selection of a preferred keyboard remains in any case one of choice and has no particular bearing on the teachings of the invention.

Because of the "slow" realtime key function selection by an operator in comparison to the "fast" processing speed of even the slower control processor, the interpretation of which key function has been selected may be made by the control processor 49. An "event" indication character communicated to the application processor 48 preferably reflects already which of the available functions of a particular key has been selected. The preprocessing of relatively slow occurring events has been found to limit the operational periods of the application processor 48.

The control processor further controls an input to an audible alarm circuit 63 ("BUZZER"). An audible alarm is a "slow occurring event" which alerts an operator of an alarm condition or signals that a processing operation has been completed. For example, when the application processor 48 has received a string of data from a bar code via the scanner module 41, and has further processed the received information to verify its correctness, the application processor 48 may communicate an acceptance code to the control processor 49 and be shut down from further operation. The control processor will then routinely generate an audible signal to alert the operator of the acceptance of the information. Prior to communicating the acceptance code to the control processor, the application processor may retrieve from its memory 57, for example, further information relating to the

bar code information which has just been read and accepted, and may compile an information screen displaying such retrieved further information to the operator prior to the deactivation of the application processor 48. Thus, by the time the operator is alerted by the audible signal that the respective bar code information has been read and accepted, the pertinent further information relating to the bar code information is already displayed on the LCD display screen 20.

Another device which is preferably under direct control of the control processor 49 is the power control circuit 64 ("CHARGE/POWER CONTROL") of the terminal unit 10. A serial interface 34 may optionally be controlled by the control processor 49. Based on the power saving interaction between the application processor 48 and the control processor 49, various additions of other devices or functions to the general operation of the terminal unit 10 may be feasible without unduly limiting the operational cycle of the terminal unit 10.

The interaction between the control processor 49 and the application processor 48 is described in greater detail in reference to FIG. 2. In general, the application processor is restricted to data processing operations. The operations of the control processor 49 generally pertain to input-output control functions which include periodic monitoring functions, such as monitoring the state of the battery 23 via the charge/power control circuit 64. Though less powerful and slower than the application processor 48, the control processor 49 controls the activation or reactivation of the application processor 48. However, the application processor 48 preferably processes the parameters and feeds the respective instructions by which the control processor is operated to the control processor 49.

Changes may be made in the selection of the first and second microprocessor devices 48 and 49 as application and control processors, respectively. The described microprocessor devices have been found particularly suitable for various operations that were expected to be performed by the terminal unit 10 in the above-referred to operations.

It should be realized that, depending on the contemplated type of portable use, various other changes and modifications in the structure of the described embodiment would be possible without departing from the spirit and scope of the invention as set forth in the claims.

IN THE CLAIMS:

1. In a portable data collection terminal unit, a data communication and processing arrangement comprising:

a plurality of distinct functional units each unit performing a predetermined function including keyboard input signalling, display screen data presentation, data processing, battery power monitoring, radio transceiver data transmissions and receptions;

means for communicating data messages among the distinct functional units, the communication means including terminal elements at each of the functional units; and

means for selectively activating the terminal elements at two of the functional units for communicating data between the two functional units and for deactivating the activated terminal elements upon conclusion of the communication of data between the two functional units.

2. The data communication and processing arrangement according to claim 1 wherein the means for communicating data messages comprises:

a control unit, the control unit being one of the distinct functional units;

a data bus extending between the control unit and other of the distinct functional units;

a plurality of microprocessors, each disposed at one of the other functional units and coupled to the data bus to form a data bus terminal at the respective functional unit; and

a control processor disposed at the control unit, coupled to the data bus and including means for controlling communication over the data bus.

3. The data communication and processing arrangement according to claim 2, the control unit further comprising an application processor communicatively coupled to the control processor for performing data processing operations, the control unit further including means for deactivating the application processor at the conclusion of a data processing operation, the control processor including means for activating the application processor on the occurrence of an event requiring data processing operations by the application processor, whereby the application processor is activated intermittently solely to perform data processing operations and remains deactivated during other periods.

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Fig.1

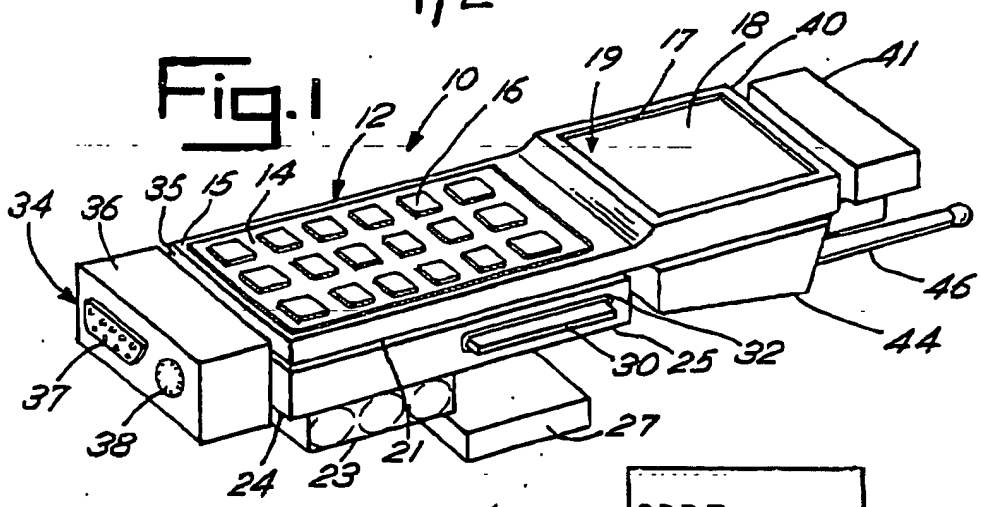

Fig.3

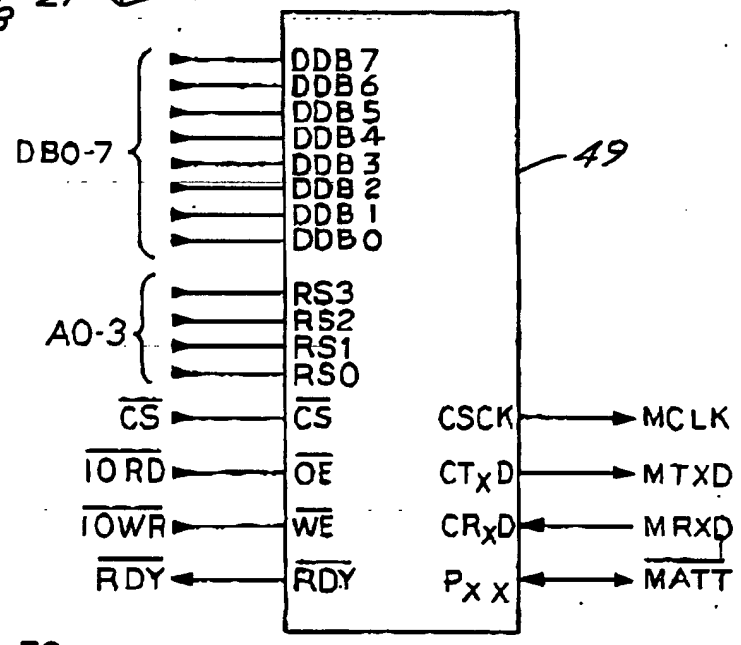

Fig.4

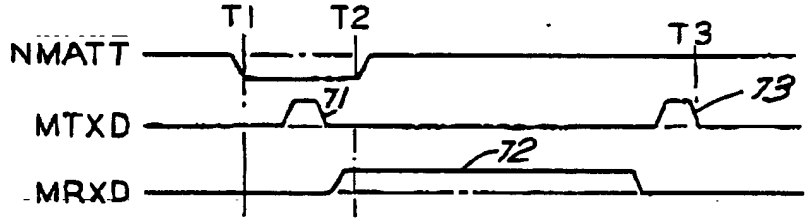

Fig.5

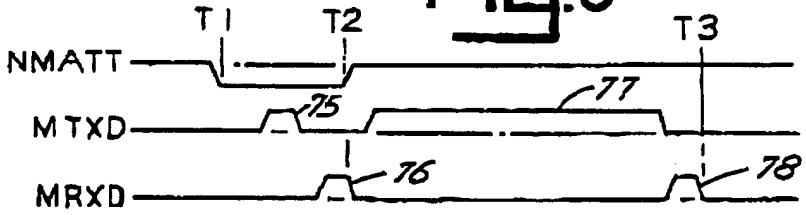

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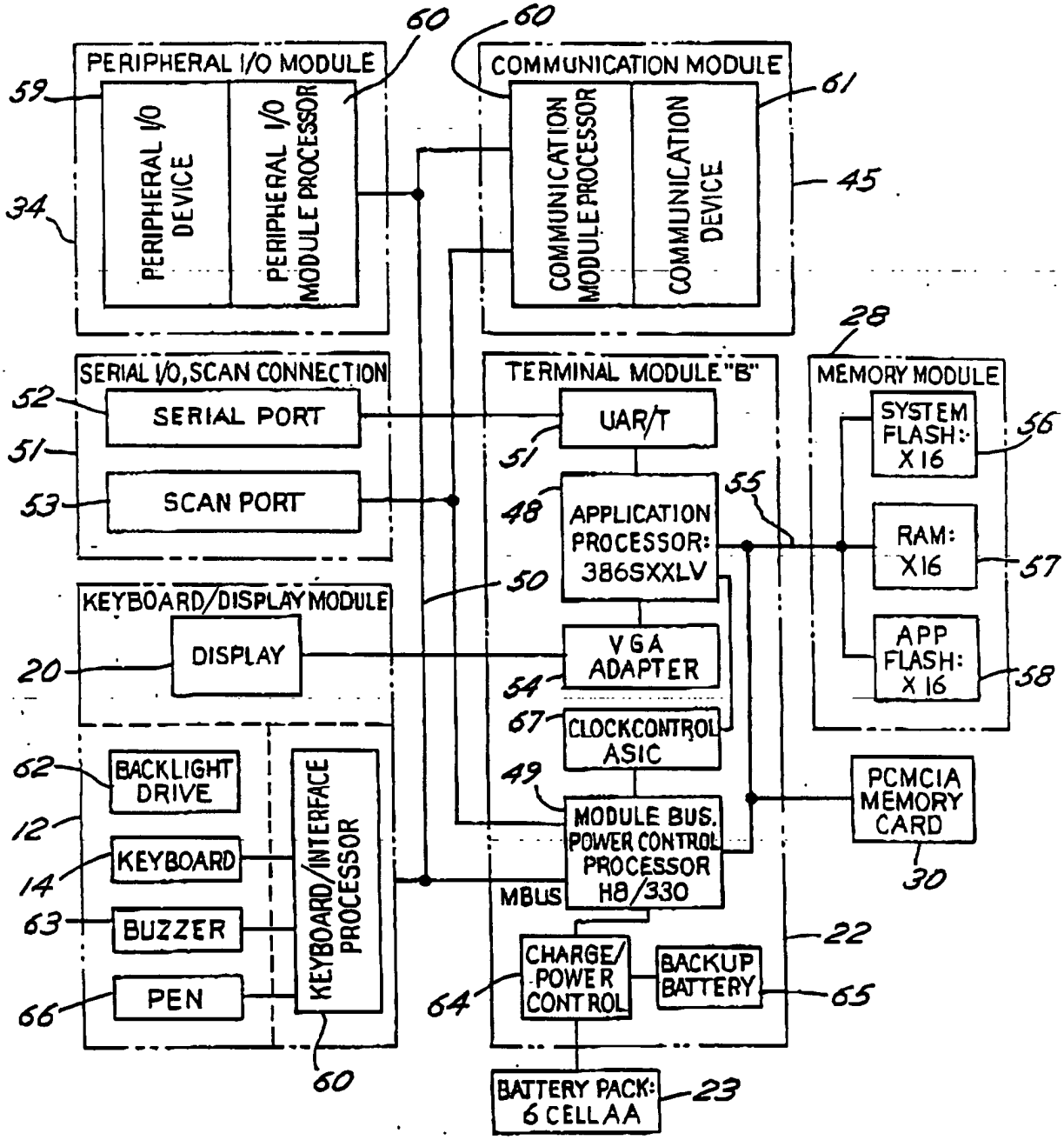
Fig.2


PERIPHERAL I/O MODULE
PERIPHERAL I/O DEVICE
PERIPHERAL I/O MODULE PROCESSOR
COMMUNICATION MODULE
COMMUNICATION MODULE PROCESSOR
COMMUNICATION DEVICE
SERIAL I/O, SCAN CONNECTION
SERIAL PORT
SCAN PORT
TERMINAL MODULE "B"
UART
APPLICATION PROCESSOR: 386SXXLV
VGA ADAPTER
CLOCKCONTROL ASIC
MODULE BUS. POWER CONTROL PROCESSOR H8/330
MBUS
CHARGE/ POWER CONTROL
BACKUP BATTERY
BATTERY PACK: 6 CELL AA
MEMORY MODULE
SYSTEM FLASH: X16
RAM: X16
APP FLASH: X16
PCMCIA MEMORY CARD
KEYBOARD/DISPLAY MODULE
DISPLAY
BACKLIGHT DRIVE
KEYBOARD
BUZZER
PEN
KEYBOARD/INTERFACE PROCESSOR
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34
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INTERNATIONAL SEARCH REPORT

International application No.
PCT/US93/05648

A. CLASSIFICATION OF SUBJECT MATTER

IPC(5) :Please See Extra Sheet.
US CL :395/750, 800
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 395/750, 800

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

Please See Extra Sheet.

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y,P	US,A ,5,142,684 (Perry et al) 25 August 1992,figs.2,3,col.2,lines 20-63, and col. 5,line 11-col.6,line 62.	1-3
Y	US,A, 4,952,817 (Bolan et.al.) 28 AUGUST 1990 figs. 1,2, col.2,line 27-col. 3,line 40.	1-3
Y	US,A, 4,649,491(Manduley) 10 March 1987, figs.1,3,4,5, col.1,lines 44-66 and col. 7,lines 2-38.	1-3

[X] Further documents are listed in the continuation of Box C. [ ] See patent family annex.

*	Special categories of cited documents:	"T"	later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"A"	document defining the general state of the art which is not considered to be part of particular relevance	"X"	document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"E"	earlier document published on or after the international filing date	"Y"	document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"L"	document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"&"	document member of the same patent family
"O"	document referring to an oral disclosure, use, exhibition or other means		
"P"	document published prior to the international filing date but later than the priority date claimed		

Date of the actual completion of the international search	Date of mailing of the international search report 20 SEP 1993
Name and mailing address of the ISA/US Commissioner of Patents and Trademarks Box PCT Washington, D.C. 20231 Facsimile No.	Authorized officer Eric Coleman ERIC COLEMAN EXAMINER ART UNIT 232 230 Telephone No.

Form PCT/ISA/210 (second sheet)(July 1992)*

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US93/05648

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US,A 5,058,203, (Inagami) 15 October 1991, figs. 1,2,3, col. 3,lines 23-46,col.4,lines 40-50.	1-3
A	US,A, 4,545,030(Kitchin) 1 October 1985 fig.1, col. 2,lines 16-39.	1-3
A	US,A, 4,545,030(Kitchin) 1 October 1985 fig.1, col. 2,lines 16-39. 1-3	

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US93/05648

A. CLASSIFICATION OF SUBJECT MATTER:
IPC (5):

G06F 1/32, 15/16

B. FIELDS SEARCHED
Electronic data bases consulted (Name of data base and where practicable terms used):

APS USPAT FILE
search terms: portable, hand-held, laptop, miniature, lightweight, microprocessor, microcomputer, power down, conserve power, power reduction, cutoff power, shutdown power, bus